



**Silicon Motion, Inc.**

## **SM3260 Test Program and ISP Release Note**

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Release Date	ISP Version	ISP Check Sum	Test AP Version	Description
2011/12/09	111209-AB-	SM3260ABPTEST.BIN SM3260ABISP.BIN 0x00800A07 SM3260ABISP-27nm.BIN 0x 00800A07	V 2.3.60 v8 11/12/09Build	<ol style="list-style-type: none"> <li>1. First 3260 MP tool release for new</li> <li>2. Support IM L74 SDR and DDR mode.</li> <li>3. Support Samsung 27nm MLC flash SDR and DDR mode.</li> <li>4. SM325Xtest.exe support SM3260 IC version.</li> </ol>
2012/01/05	111229-AB	SM3260ABISP.BIN 0x00810F79 SM3260ABISP-27nm.BIN 0x00810F79 SM3260ABISP-Toshiba.BIN 0x00810F79	V 2.3.62 v9 11/12/26Build	<ol style="list-style-type: none"> <li>1. SM3260 Pretest support "erase info" for flash change mode.</li> <li>2. SM3260 Pretest fixed "Erase Good block only" will show wrong bad block number.</li> <li>3. SM3260ISP support Samsung 27nm TLC.</li> <li>4. SM3260ISP modified the error handling when block have ECC fail on link table/FAT table.</li> <li>5. MP tool support "Windows7 factory driver"</li> </ol>
2012/01/20	120120-AB	SM3260ABISP.BIN 0081C680 SM3260ABISP-27nm.BIN 0081C680 SM3260ABISP-Toshiba.BIN 0081C680 SM3260ABISP-L84.BIN 0081C680	V 2.3.65 v4 12/01/16Build	<ol style="list-style-type: none"> <li>1. Support Sandisk / Toshiba 24nm MLC</li> <li>2. Support Toshiba 19nm MLC.</li> <li>3. Support Intel &amp; Micron 20nm SDR/DDR MLC L84A.</li> <li>4. Adjust USB clock rate to 120 MHz for Toggle Flash</li> <li>5. Update the MP tool version for SM3260AC</li> </ol>



2012/02/15	120208-AB	SM3260ABISP.BIN 0081E75F SM3260ABISP-27nm.BIN 0081E75F SM3260ABISP-24nm.BIN 0081E75F SM3260ABISP-L84.BIN 0081E75F SM3260ABISP-SA21nmMLC.BIN 0081E75F	V 2.3.66 v4 12/02/03Build	<ol style="list-style-type: none"> <li>1. Fix Suddenly Power cycling Issue</li> <li>2. Support Samsung 21nm DDR MLC.</li> </ol>
2012/04/07	120406-AB 120406-AD	SM3260ABISP-ISPT24nm.BIN 008180B0 SM3260ABISP-ISPSD24nm.BIN 008180B0 SM3260ADISP-ISPT24nm.BIN 0081AF5B SM3260ADISP-ISPSD24nm.BIN 0081AF5B	V 2.3.69 v9 12/04/06 Build	<ol style="list-style-type: none"> <li>1. Support Toshiba TC58NVG4D2HTA00 24nm MLC.</li> <li>2. Support only 1 LED Setting</li> <li>3. Support Sandisk 24nm MLC.</li> <li>4. Support Samsung 21nm MLC with 4Plane mode.(K9GCGD8U0M/K9GCGD8U0A)</li> <li>5. Support TSB &amp; SDK 24nm TLC with 2c1w mode. (SDTNPAHEM-008G / TC58TVG5T2HTA00 / TC58TVG6T2HTA00)</li> <li>6. Add Samsung 27nm MLC read-retry table.</li> </ol>
2012/04/20	120417-AB 120418-AD	SM3260ABISP-ISPT24nm.BIN 0080EB6E SM3260ABISP-ISPSD24nm.BIN 0080EB6E SM3260ABISP-ISPT19nm.BIN	V 2.3.70 v8 12/04/18 Build	<ol style="list-style-type: none"> <li>1. Supports SanDisk / Toshiba 19nm SDR TLC 64Gb.</li> <li>2. Supports SanDisk / Toshiba 24nm TLC 2CH1W/2CH2W mode.</li> <li>3. Modify 24nm/ 19nm U2/U3 busy stat LED behavior.</li> <li>4. Support TLC block WAI function.</li> <li>5. Fix 1K read-retry issue.</li> </ol>



		0080EB6E SM3260ABISP-ISPSPD19nm.BIN 0080EB6E SM3260ADISP-ISPT24nm.BIN 008121C4 SM3260ADISP-ISPSPD24nm.BIN 008121C4 SM3260ADISP-ISPT19nm.BIN 008121C4 SM3260ADISP-ISPSPD19nm.BIN 008121C4		
2012/05/08	120503-AB 120508-AD	SM3260ABPTEST.BIN 008192EA SM3260ABISP.BIN 008192EA SM3260ABISP-27nm.BIN 008192EA SM3260ABISP-24nm.BIN 008192EA SM3260ABISP-B74.BIN 008192EA SM3260ABISP-L84.BIN 008192EA SM3260ABISP-SA21nmMLC.BIN	V 2.3.73 v6 12/05/08 Build	<ol style="list-style-type: none"> <li>1. Support 4K SLC flash: K9WBG08U1M / JS29F64G08JCND1 / JS29F16B08HCND1</li> <li>2. Support Micron L84A with Cache Read/Program and support 2c4w mode.</li> <li>3. Support SDK/TSB 19nm 64Gb SDR / DDR 2Ch 1Way</li> <li>4. Support SDK/TSB 19nm 128Gb SDR / DDR 2Ch 1Way</li> </ol>



		008192EA SM3260ADISP.BIN 007FF0F5 SM3260ADISP-27nm.BIN 007FF0F5 SM3260ADISP-24nm.BIN 007FF0F5 SM3260ADISP-B74.BIN 007FF0F5 SM3260ADISP-L84.BIN 007FF0F5 SM3260ADISP-SA27nmMLC.BIN 007FF0F5 SM3260ADISP-SA21nmMLC.BIN 007FF0F5		
2012/06/12	120612-AD	SM3260ADISP-SA21nmMLC4P.BIN 00803C11 SM3260ADISP-19nm16K.BIN 0082290E SM3260ADISP-ISPT24nm.BIN 0081E2BB SM3260ADISP-IPSPD24nm.BIN 0081E2BB	V 2.3.80 v5 12/06/12 Build	<ol style="list-style-type: none"> <li>1. Support SEC 27nm 16Gb MLC K9GAG08U0F</li> <li>2. Support SEC 21nm 64Gb MLC K9GCGD8U0A</li> <li>3. Support SanDisk 19nm 64Gb 16K 2Plane MLC SDTNQGAMA-008G</li> <li>4. Update Toshiba 19nm TLC retry table parameter.</li> <li>5. Supports new BCT table mechanism for DDR flash</li> <li>6. Fix performance drops with HDBench.</li> <li>7. MPTool support "Card mode check mechanism"</li> </ol>



		SM3260ADISP-ISPSA21nm.BIN 0081E2BB SM3260ADISP-ISPT19nm.BIN 0081E2BB SM3260ADISP-ISPSD19nm.BIN 0081E2BB SM3260ADISP-ISPT19nm4P.BIN 008293C9 SM3260ADISP-ISPSD19nm4P.BIN 008293C9		8. MPtool resolve "Card mode calculate wrong issue for multiple devices" 9. MPTool support copy compare function with clean pattern, write only and read only options. 10. MPTool support "Check all same flash type and CE numbers" during MP.
2012/07/26	19/21/24nmTLC: 120719-AD Others: 120726-AD	SM3260ADTSPTEST.BIN 0x4B57C3 SM3260ADISP-ISPT24nm.BIN 00827532 SM3260ADISP-ISPSD24nm.BIN 00827532 SM3260ADISP-ISPSA21nm.BIN 00827532 SM3260ADISP-ISPT19nm.BIN 00827532 SM3260ADISP-ISPSD19nm.BIN 00827532 SM3260ADISP-ISPSD19nmDDR.BIN 00827532	V 2.3.86 v6 12/07/24 Build	1. Support Samsung 21nm TLC K9ACGD8U0A 2Ch 1 Way, 2Ch 2Way. 2. Support SDK/TSB 19nm 64Gb SDR / DDR 2Ch 2Way (SDTNQCAMA-008G / TC58NVG6T2JTA00 / TC58TEG6T2JTA00) 3. Support SDK/TSB 19nm 128Gb SDR / DDR 2Ch 2Way (SDTNQCAMA-016G / TC58NVG7T2JTA00 / TC58TEG7T2JTA00) 4. Support Intel 25nm MLC (29F64G08ACME2/29F16B08CCME2) 5. Support TSB 19nm 16K 2Plane MLC (TC58TEG6DDJBA4C) 6. Syncs SDK/TSB 19nm 4plane TLC S3 behavior with 2Plane mode can solve S3 current issue 7. Modify Samsung 21nm GCG-A die 4plane CacheProgram flow. 8. Adjust driving current for Toshiba & Sandisk 24nm/19nm TLC



		SM3260ADISP-ISPT19nm4P.BIN 0082E1D6 SM3260ADISP-ISPSD19nm4P.BIN 0082E1D6 SM3260ADISP-ISPSD19nm4PDDR.BIN 0082E1D6 SM3260ADPTEST.BIN 0x60927F SM3260ADISP.BIN 00801CAA SM3260ADISP-27nm.BIN 00801CAA SM3260ADISP-24nm.BIN 00801CAA SM3260ADISP-B74.BIN 00801CAA SM3260ADISP-L84.BIN 00801CAA SM3260ADISP-SA27nmMLC.BIN 00801CAA SM3260ADISP-SA21nmMLC.BIN 120726-AA		with 1way. 9. Define CID 0x161 bit3 to prevent FW write protect function for SM3260AD with 19/21/24nm TLC flash. (default disable) 10. Fix Crystal Disk Mark 500MB sequential write performance unstable issue 11. Support Samsung 21nm MLC K9GCGY8S0A with 4-plane mode for SM3260AD. 12. Update Samsung 21nm read retry flow.
2012/08/30	120827-AD	SM3260ADISP-19nm16K.BIN	V 2.3.90 v5	1. Update Samsung 21nm GCG-A die / disable cache program



		008200A3 SM3260ADISP-ISPT24nm.BIN 00823C9A	12/08/24 Build	<ol style="list-style-type: none"> <li>2. Support Hynix 20 nm UCG-A die, H27UCG8T2ATR (8K / 2Plane)</li> <li>3. Support Hynix 20 nm UCG-B die, H27UCG8T2BYR (16K / 2Plane)</li> <li>4. Support Samsung 32nm MLC K9PFGD8U5M</li> <li>5. Support Samsung 32nm SLC K9KBGD8U1M / K9WCG08U5M / K9QDG08U5M</li> <li>6. Improve error handling for SPOR (19nm TLC / 21nm TLC / 24nm TLC)</li> <li>7. Support Toshiba 19nm TLC SDR mode to DDR mode. (Flash ID 6th 0x57 will not be changed)</li> <li>8. Force Sandisk 19nm TLC SDR mode to DDR mode. (Flash ID 6th 0x57 will not be changed).</li> <li>9. Adjust the clock rate to 99MHz for Sandisk and Toshiab 19nm SDR MLC.</li> </ol>
2012/10/12	121012-AD	SM3260ADISP.BIN 00819C5B SM3260ADISP-ISPT19nm.BIN 0082466C SM3260ADISP-ISPT19nm4P.BIN 0082A6D1 SM3260ADISP-ISPSD19nm4P.BIN 0082A6D1	V 2.3.96 v2 12/10/12 Build	<ol style="list-style-type: none"> <li>1. Disable GCG-A die cache program</li> <li>2. Update LED Flash behavior (default support location D1 only)</li> <li>3. Fix Hynix UCG B die fixed capacity issue</li> <li>4. Update Micron L84A read retry flow</li> <li>5. Update Micron 25nm L74 DDR with Read 132 / Write 120MHz</li> <li>6. Update Micron 25nm M73 DDR with Read 132 / Write 120MHz</li> </ol>





				<ul style="list-style-type: none"> <li>7. Support Toshiba 24nm MLC with SDR to DDR mode.</li> <li>8. Update Toshiba 24nm MLC DDR with Read 132 / Write 120Mhz</li> <li>9. Fine-tune 19nm TLC FW to improve SPOR issue</li> </ul>
2012/11/01	121101-AD	SM3260ADISP.BIN SM3260ADISP-L84.BIN SM3260ADISP-24nm.BIN 0081BA73 SM3260ADISP-19nm16K-HY.BIN 0081D0C9	V 2.3.98 v4 12/10/25 Build	<ul style="list-style-type: none"> <li>1. Modify the LED blinking setting.</li> <li>2. Fine Tune FW for SPOR test</li> <li>3. Fix plug in/out then performance drop issue</li> <li>4. Modify the Read retry flow under DDR mode</li> <li>5. Fix 20nm Hynix UCG-B die Card Mode issue</li> </ul>
2012/11/13	121113-AD	SM3260ADISP.BIN 0081F939 SM3260ADISP-ISPT24nm.BIN 00824BE1 SM3260ADISP-ISPSA21nm.BIN 00824BE1 SM3260ADISP-ISPT19nmDDR.BIN 00824BE1 SM3260ADISP-ISPT19nm4P.BIN 00829243 SM3260ADISP-ISPT19nm4PDDR.BIN 00828CF1	V 2.5.01 v8 12/11/12 Build	<ul style="list-style-type: none"> <li>1. Update LED blinking setting for 19/21/24nm TLC (default setting: Both D1/D2 will be blinking in both U2/U3 mode)</li> </ul>



2012/12/07	121206-AD	SM3260ADISP.BIN 0081DCB1	V 2.5.04 v3 12/12/05 Build	<ol style="list-style-type: none"><li>1. Fine tune WinSAT performance for L84A/B74A.</li><li>2. Improve Samsung 21nm TLC / Toshiba 129nm TLC / SanDisk 19nm TLC Read Performance.</li></ol>
2013/01/24	130118-AD	SM3260ADISP.BIN	V 2.5.10 v6 13/01/17 Build	<ol style="list-style-type: none"><li>1. Fix suspend/resume drop issue</li><li>2. Update Samsung 21nm MLC Read-Retry Table.</li><li>3. Update Sandisk 19nm MLC Read-Retry Table.</li><li>4. Fix LPM issue for USB3 suspend.</li><li>5. Fine tune WinSAT performance for Hynix 20nm MLC</li></ol>
2013/03/15	130315-AD	SM3260ADISP.BIN SM3260ADISP-L85.BIN	V 2.5.15 v1 13/03/04 Build	<ol style="list-style-type: none"><li>1. Modify/enhance Samsung 21nm TLC read-retry.</li><li>2. Support I/M 20nm 128Gb MLC L85 x4 / x8: MT29F128GCBCAB / JS29F16B08LCMF3</li></ol>
2013/04/03	130329-AD	SM3260ADISP.BIN	V 2.5.16 v3 13/03/26 Build	<ol style="list-style-type: none"><li>1. Adjust PHY setting to solve the Read/Write Reset when Power Drop.</li><li>2. Support PHY setting select by DBF</li><li>3. Improve cache table block error handling.</li></ol>