



SD-PWS Link

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Introduction

This special training <Link between System Designer and PWS> describes operation flow between System Designer and PWS.

This text focuses on precautions and restricted matters for link between System Designer and PWS. For detailed operation of System Designer and PWS, please refer to each their respective training manuals.

<System Designer>

CR-5000 System Designer Operation Guide - BEGINNER -
CR-5000 System Designer Operation Guide - MASTER -

<PWS>

PWS for UNIX or PWS for Windows
<Net operation>
<Design modification>

This text is described based on the following version.

*System Designer ... Rev.6.0

*PWS ... Rev.12.1

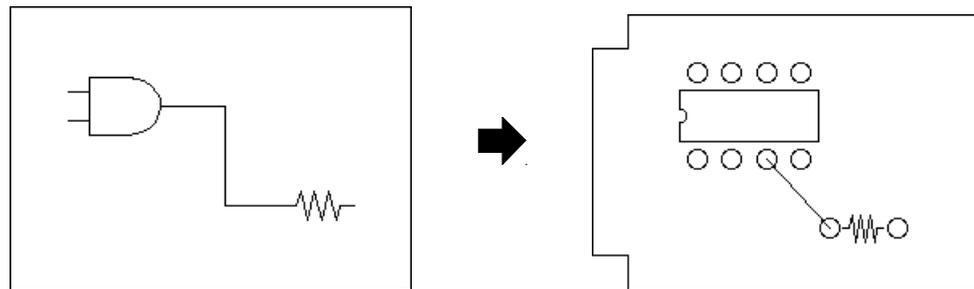
1.Function Overview

This section shows operation flow of designing board in PWS according to information of circuit data designed in System Designer.

The following functions are available for link between System Designer and PWS.

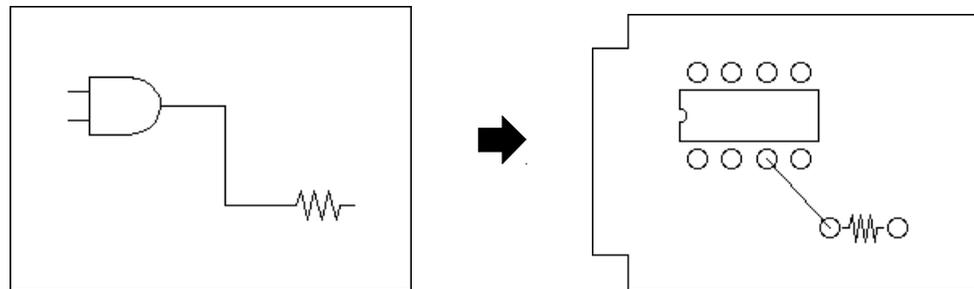
***Forward annotation**

Designs a board in PWS depending on information of a circuit data designed in System Designer.



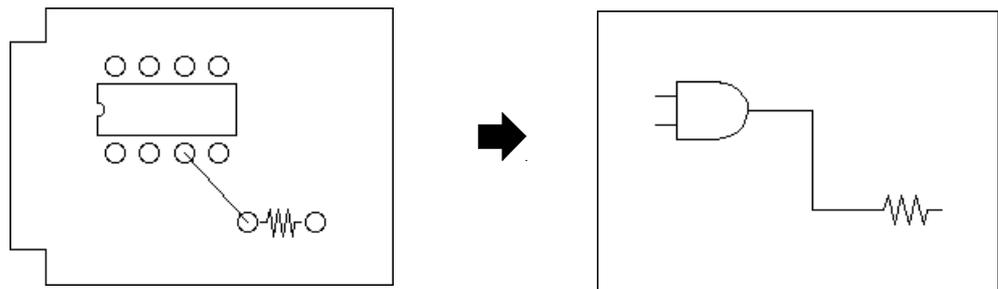
***Modifying design**

Applies modified circuit information to a board which is being edited or has been completed.

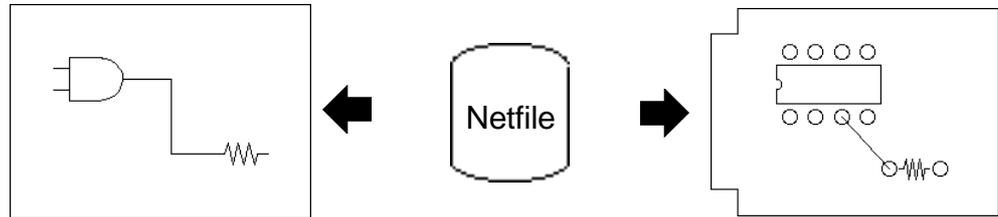


***Back annotation**

Applies modified circuit information, which was done by gate exchange in PWS, etc., to original circuit data.



On “Link between System Designer and PWS”, transfer of all information is done via net file.



The following 4 files are prepared for performing “Link between System Designer and PWS”.

- *Circuit mark net file (Without DEFINITION section) CCF
- *Circuit mark net file (With DEFINITION section) CCF
- *Extended circuit mark net file ECF
- *Gate net file GNF

Available functions and required library vary depending on net type.

	Forward annotation	Design modification	Back annotation	Pmaster (library)
CCF without DEF	Available	Available	Not Available	Not required
CCF with DEF	Available	Available	Not Available	Required
ECF	Available	Available	Available	Required
GNF	Available	Available	Available	Required

2.Net File Type

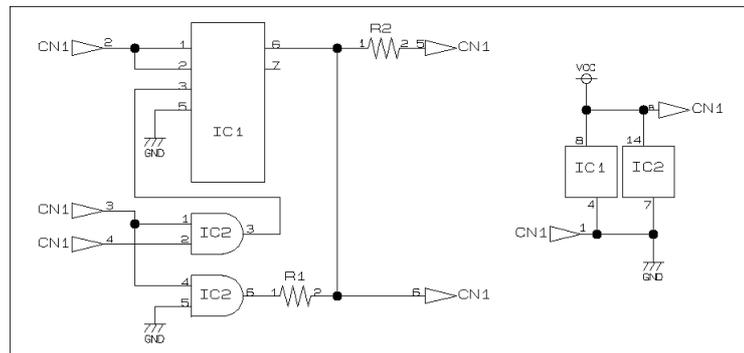
This section describes 4 nets format type that can be transferred between System Designer and PWS.



Net files described here have some sections except items described here, however, they cannot be outputted from System Designer.

*Circuit mark net file (Without DEFINITION section) CCF

Circuit mark net file is a net file that represents connection depending on information of references and pin numbers.



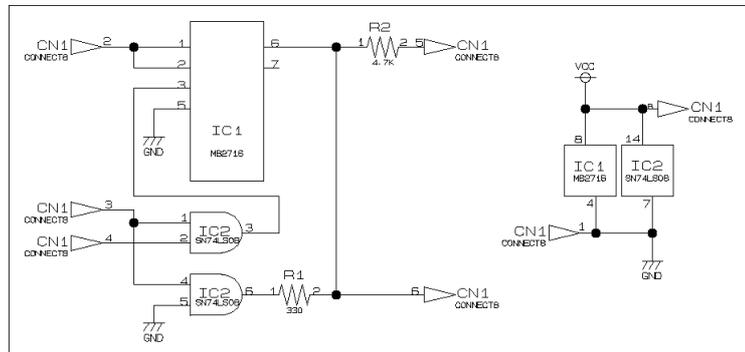
```

$CCF {
NET {
    SIGN1: CN1(2),IC1(1),IC1(2);
    NetName:Reference(PinNumber),Reference(PinNumber), - - -;
    SIGN2: CN1(4),IC2(2);
    SIGN3: CN1(3),IC2(1),IC2(4);
    SIGN4: IC1(3),IC2(3);
    SIGN5: IC2(6),R1(1);
    SIGN6: CN1(5),R2(2);
    SIGN7: CN1(6),IC1(6),R1(2),R2(1);
}
GROUND {
    GND: CN1(1),IC1(4),IC1(5),IC2(5)
    ,IC2(7);
}
POWER {
    VCC: CN1(8),IC1(8),IC2(14);
}
ONE_STROKE_NET {
}
}
    
```



***Circuit mark net file (With DEFINITION section) CCF**

Reference and corresponding part name are described in DEFINITION section.



```

$CCF {
  DEFINITION {
    330: R1;
      PartName:Reference,Reference, - - -;

    4.7K: R2;
    CONNECT8: CN1;
    MB2716: IC1;
    SN74LS08: IC2;
  }
  NET {
    SIGN1: CN1(9),IC1(1),IC1(9);
      NetName:Reference(PinNumber),Reference(PinNumber), - - -;

    SIGN2: CN1(4),IC2(2);
    SIGN3: CN1(3),IC2(1),IC2(4);
    SIGN4: IC1(3),IC2(3);
    SIGN5: IC2(6),R1(1);
    SIGN6: CN1(5),R2(2);
    SIGN7: CN1(6),IC1(6),R1(2),R2(1);
  }
  GROUND {
    GND: CN1(1),IC1(4),IC1(5),IC2(5),IC2(7);
  }
  POWER {
    VCC: CN1(8),IC1(8),IC2(14);
  }
  ONE_STROKE_NET {
  }
}
    
```

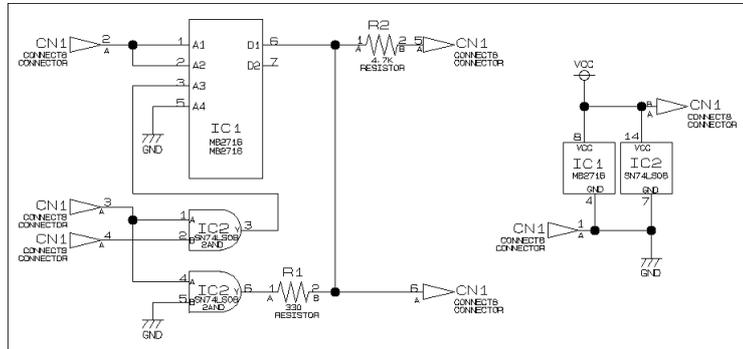
Annotations on the right side of the code block:

- File declaration (points to \$CCF {)
- DEFINITION section (points to DEFINITION {)
- Net section (points to NET {)
- Ground section (points to GROUND {)
- Power section (points to POWER {)
- One stroke section (points to ONE_STROKE_NET {)

Same as "CCF without DEF"

***Extended circuit mark net file ECF**

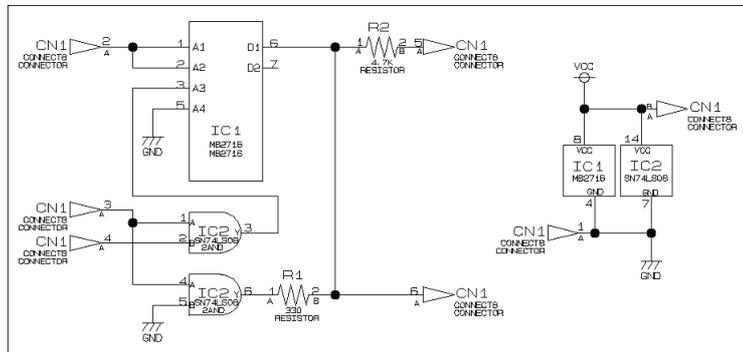
Information for each gate existing in a circuit is described in SYMBOL section.



Same as "CCF with DEF"	\$ECF {	File declaration
	DEFINITION {	DEFINITION
	330: R1;	section
	PartName:Reference,Reference,- - -;	
	4.7K: R2;	
	:	
	}	
	NET {	Net section
	SIGN1: CN1(2),IC1(1),IC1(2);	
	NetName:Reference(PinNumber),Reference(PinNumber),- - -;	
SIGN2: CN1(4),IC2(2);		
:	Ground section	
}		
GROUND {	Power section	
GND: CN1(1),IC1(4),IC1(5),IC2(5),IC2(7);		
}		
POWER {	One stroke section	
VCC: CN1(8),IC1(8),IC2(14);		
}	Symbol section	
ONE_STROKE_NET {		
}		
SYMBOL {		
1.CMP3: 2AND: IC2: B(2),A(1),Y(3);		
ComponentID:FunctionName:Reference:		
PinName(PinNumber),PinName(PinNumber),- - -;		
1.CMP4: 2AND: IC2: B(5),A(4),Y(6);		
1.CMP2: MB2716: IC1: A1(1),A2(2),A3(3)		
,A4(5),D1(6),D2(7);		
1.CMP5: RESISTOR: R1: A(1),B(2);		

***Gate net file GNF**

Connection is described for each symbol (gate) on a circuit data.



<pre> \$GNF { DEFINITION { SN74LS08:2AND: B,A,Y PartName:FunctionName:PinName,PinName,- - -; :1.CMP3,1.CMP4; :ComponentID,ComponentID,- - -; MB2716:MB2716: A1,A2,A3,A4,D1,D2 :1.CMP2; 330:RESISTOR: A,B :1.CMP5; : } GATE { 1.CMP3:IC2: SIGN2(2),SIGN3(1),SIGN4(3); ComponentID:Reference: NetName(PinNumber),NetName(PinNumber), - - -; 1.CMP4:IC2: GND(5),SIGN3(4),SIGN5(6); 1.CMP2:IC1: SIGN1(1),SIGN1(2),SIGN4(3) ,GND(5),SIGN7(6),(7); 1.CMP5:R1: SIGN5(1),SIGN7(2); : } GROUND { GND: CN1(1), IC1(4), IC1(5), IC2(5), IC2(7); NetName:Reference(PinNumber),Reference(PinNumber), - - -; } POWER { VCC: CN1(8),IC1(8),IC2(14); } ONE_STROKE_NET { } } </pre>	<p>File declaration</p> <p>DEFINITION section</p> <p>Gate section</p> <p>Ground section</p> <p>Power section</p> <p>One stroke section</p>
---	--

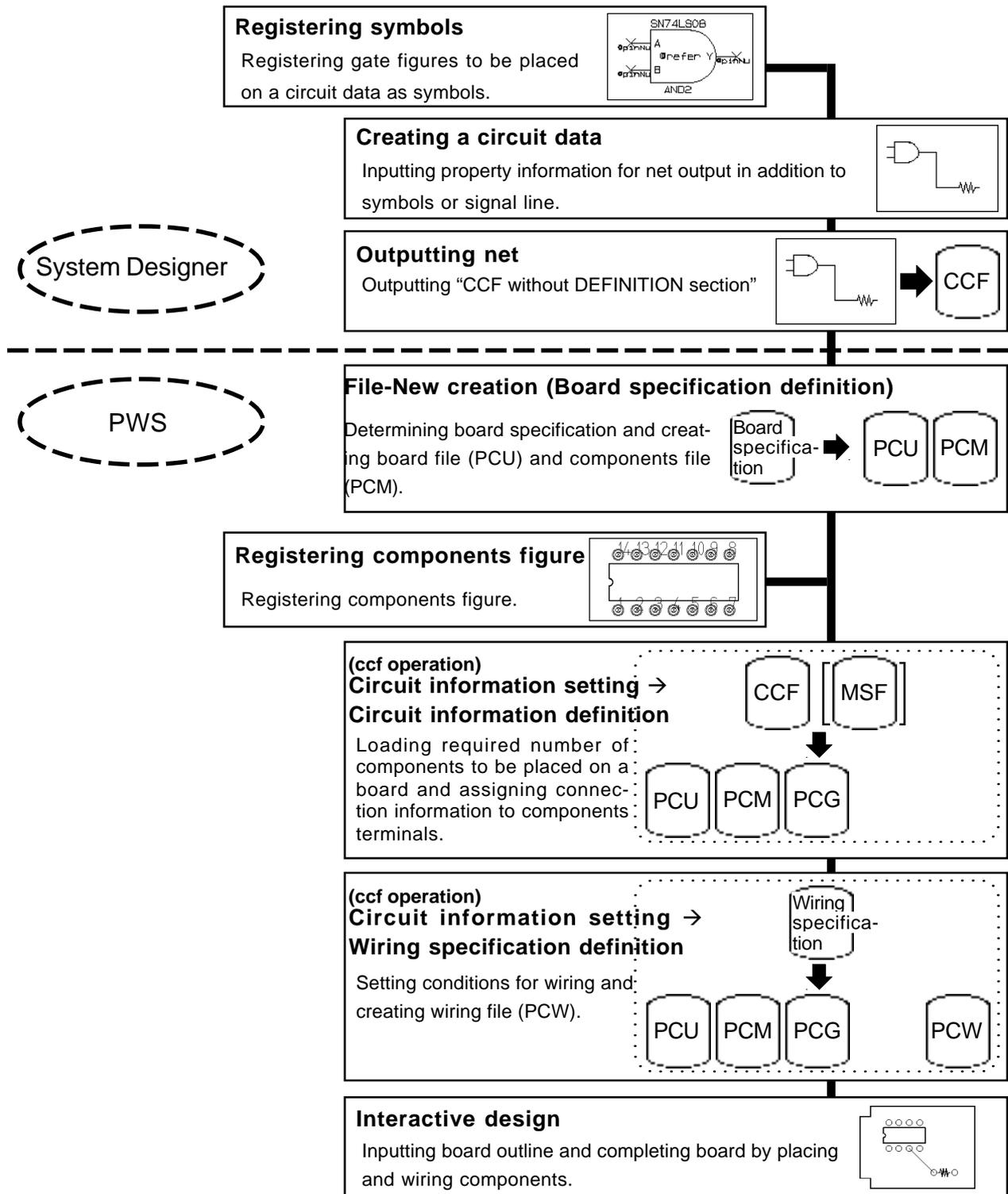
Signal name is described in order of pin name described in DEFINITION section.

3.Design Flow For Each Net

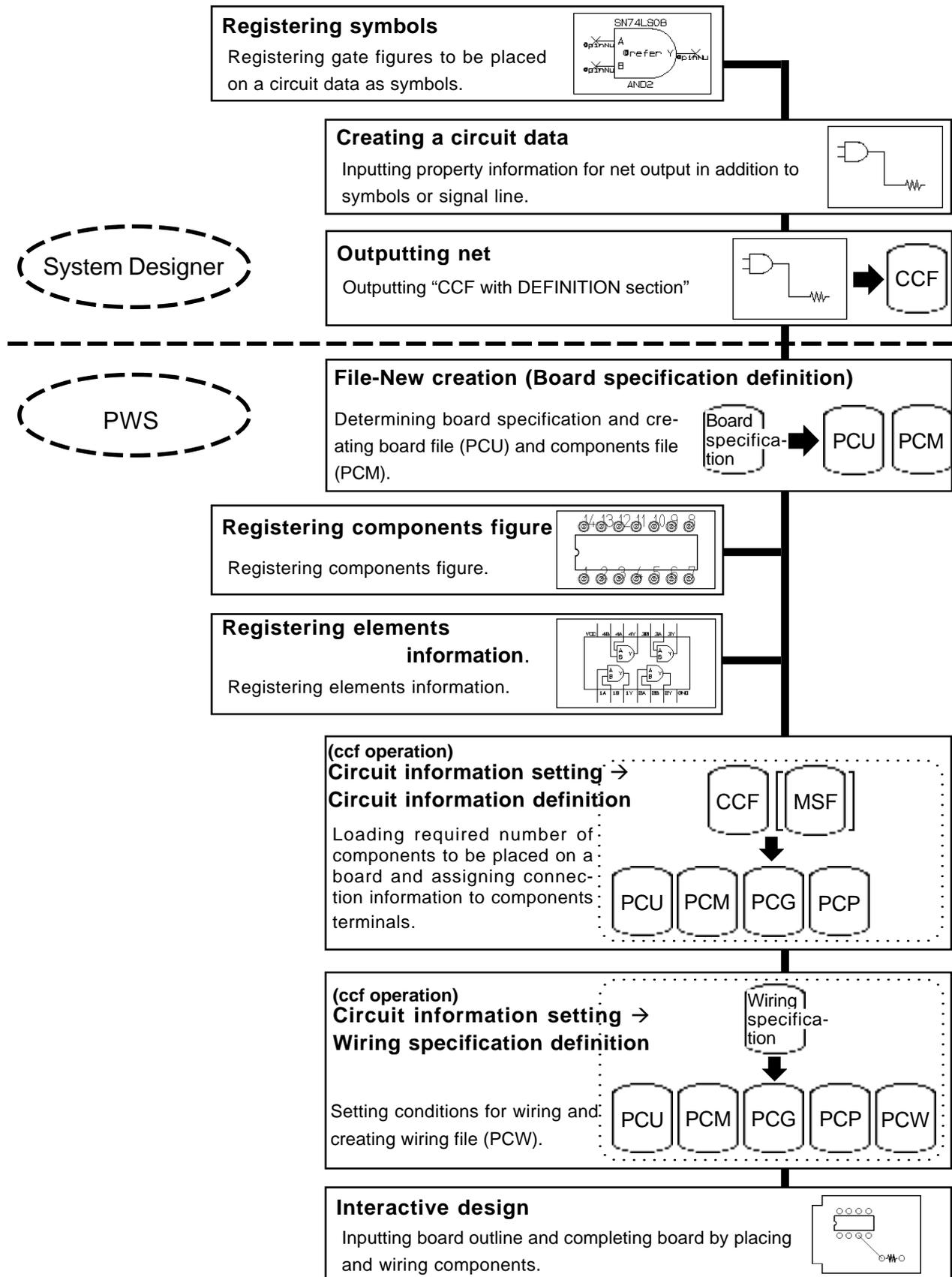
Design flow or required library vary depending on which net you choose from 4 nets type.

This section describes design flow for each net.

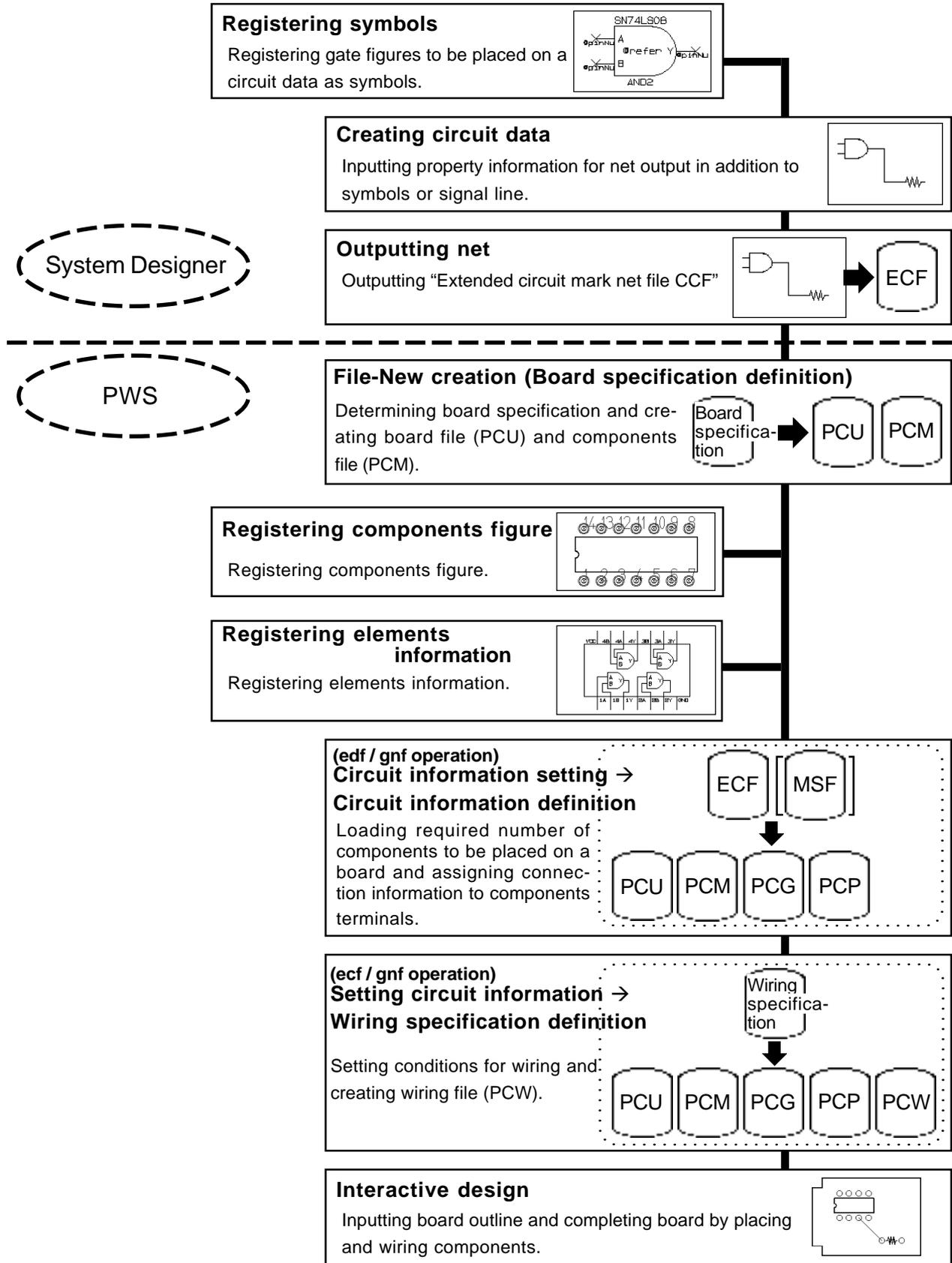
*Circuit mark net file (Without DEFINITION section) CCF



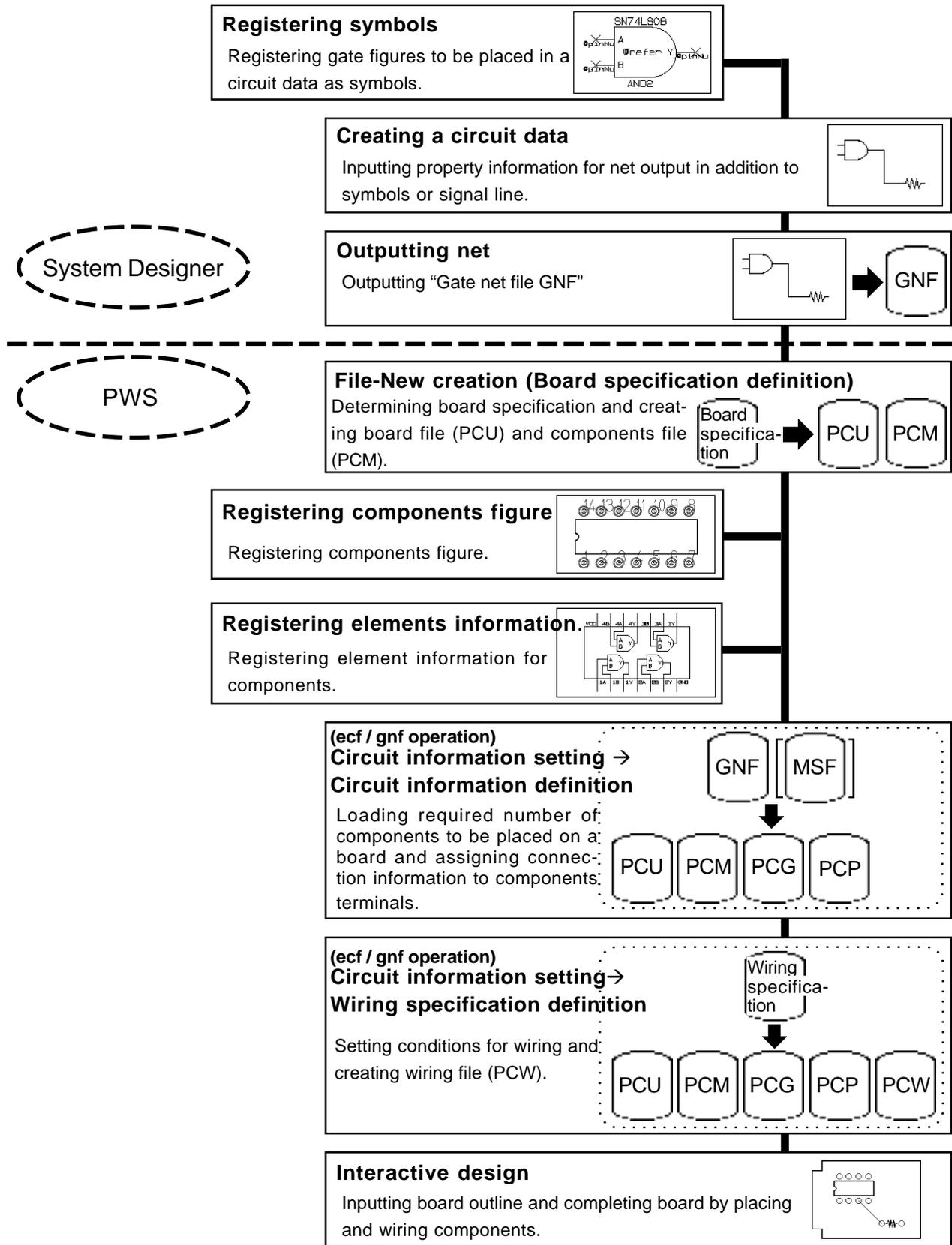
***Circuit mark net file (With DEFINITION section) CCF**



***Extended circuit mark net file ECF**



***Gate net file GNF**

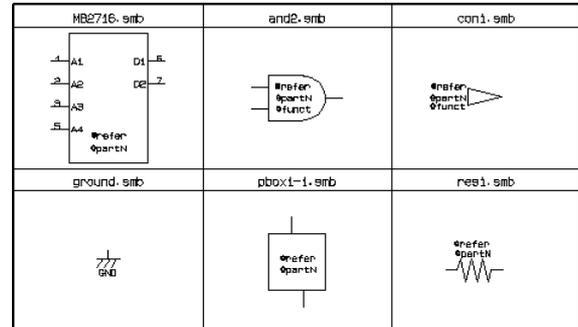


1. Registering Library

There are 2 kinds of System Designer libraries.

*Symbol library (~.smb)

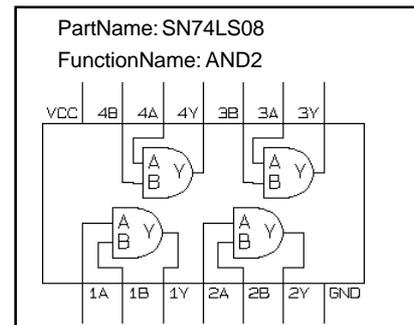
This is a library to register symbol figure. One figure is registered in one file and the file is stored in specified directory (symbol path). This is essential for creating circuit data.



*LCDB

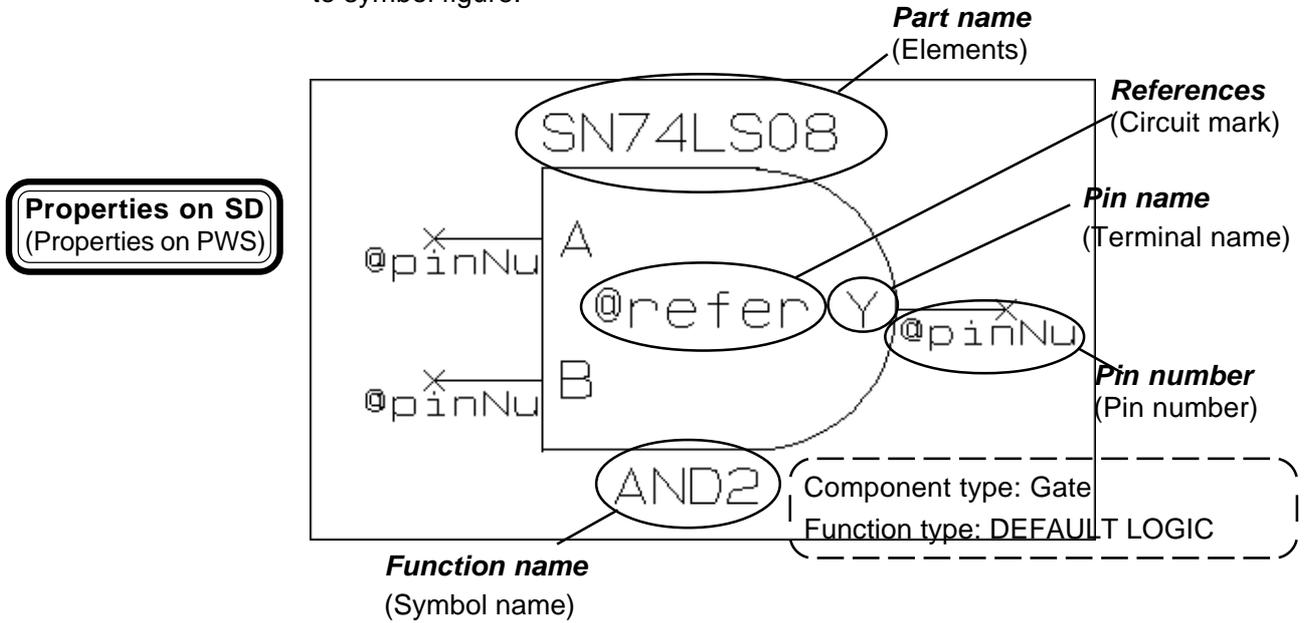
This is a library to define elements information.

One library consists of 4 files (~.prf, ~.dbf, ~.cmp, ~.rit) and information of multiple elements is stored in the library. This is essential for performing back annotation.



***Registering symbols**

On a symbol sheet, you can register properties assigned to a symbol in addition to symbol figure.



Although you can set and modify properties assigned to a symbol after being placed on a circuit sheet, it is more convenient to set predefined properties when registering symbols.

For undefined properties, you can previously set input place with property viewer(@XXXXX).

Correspondence with PWS properties

System Designer		PWS
Symbol sheet properties	Part name	Elements name
	Function name	Symbol name
Symbol pin properties	Pin name	Terminal name
	Pin number	Pin number

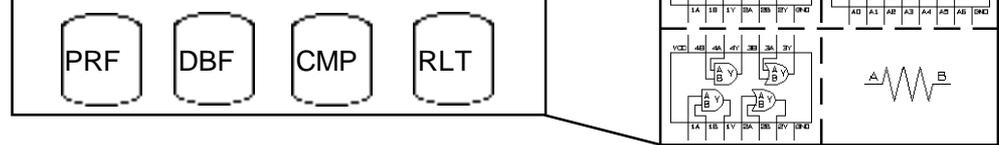


Available characters are limited in PWS. For details, refer to "Precautions for creating circuit data".

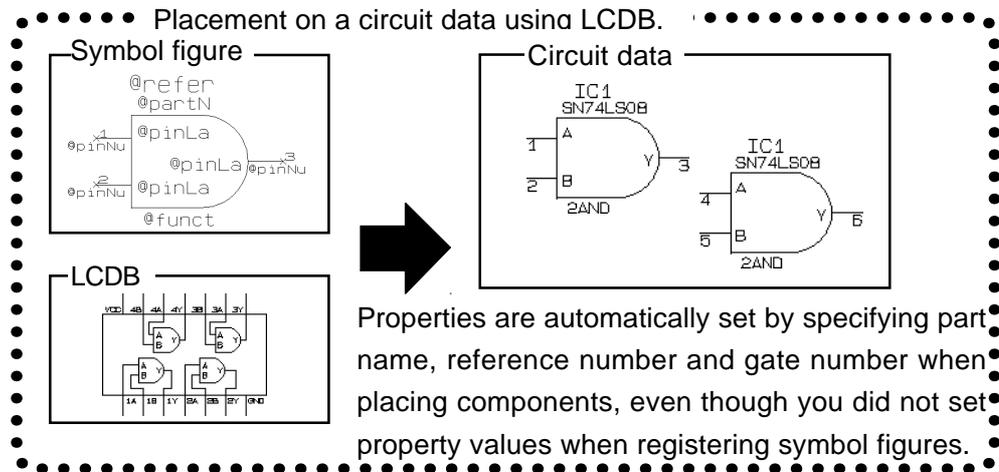
***Registering in LCDB**

LCDB is a library to define information of elements such as described in data book.

Component Database for Schematic Design.



LCDB is not especially necessary for creating a circuit data to transfer to PWS. However, it is very convenient to prepare it for creating general circuit design.



Registering in LCDB

The following properties are used for link with PWS.

Properties on SD
(Properties on PWS)

CDB Name	Part Name	Use with Layout	Component Name	Component Name	Comp
cdbName	partName	useWithLayout	componentName	componentName	comp
L2732K	L2732K	-	L2732K_package	L2732K.pbox	-
RN_A_100	RN_A_100	-	RES1_package	-	-
RN_A_330	RN_A_330	-	RES1_package	-	-
SN74LS04	SN74LS04	-	INV+8_package	INV+8_INV	INV+
SN74LS08	SN74LS08	-	ANDE+4_package	ANDE+4_AND2	AND2
SN74LS138	SN74LS138	-	SN74LS138_package	SN74LS138.pbox	-
SN74LS165	SN74LS165	-	SN74LS165_package	SN74LS165.pbox	-

Part name
(Elements name)

Function name
(Symbol name)

Pin number
(Pin number)

Pin name
(Terminal name)

Symbol Pin ID	Common Terminal?	Pin Number	Pin Label	IO
isCommonTerminal	pinNumber	pinLabel	io	
1	NO	1,3,5,9,11,13	A	INPUT
2	NO	4,6,8,10,12	Y	OUTPUT
3	YES	14	+5V	VCC
4	YES	7	GND	GND

Reference

NOTE

Reference

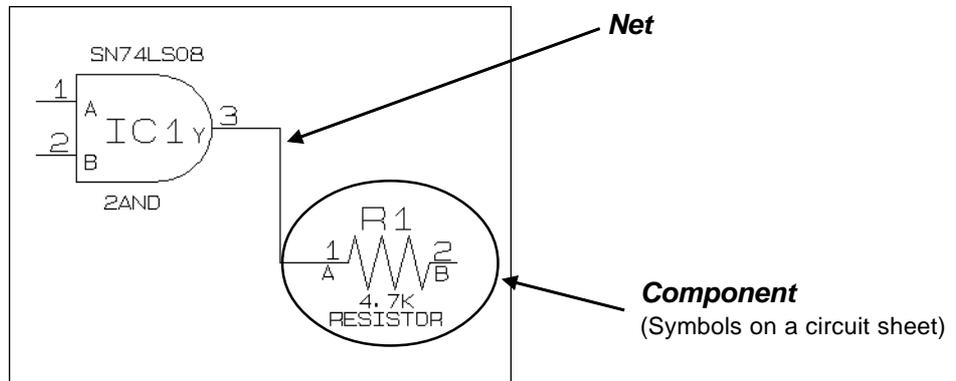
Available characters are limited in PWS. For details, refer to P2-12 "Precautions for creating circuit data".

Program to interactively convert between PWS elements information library (Pmaster) and System Designer LCDB library is provided.

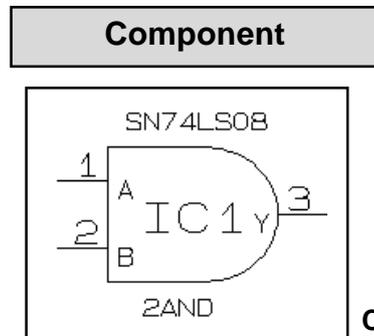
For details of converted program, refer to operation manual "LCDB-master conversion".

2. Creating circuit data

Creating circuit data by placing symbols and signal line.



For creating a circuit data for net output, make sure the following matters.



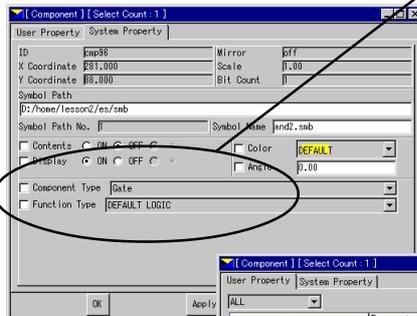
Definition of symbols to be output to net is dependent on the following 2 settings.

[Component type]
[Component properties]

Component property [Components for board design]

Component type

The following process is done for each 12 type.



Items to be output to net

Components or block. Components, Gate, Block, Gate or Block, Components or block.

Items not to be output to net

Figure, Sheet flame

Items that need special process for outputting to net.

Power, Ground...

Include connected nets in POWER and Ground section.

Short.....

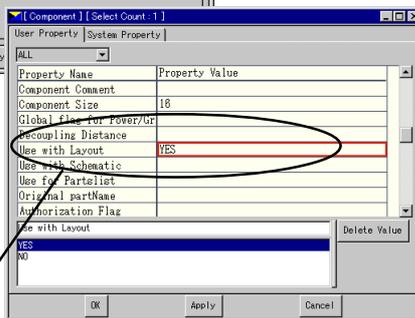
Consider that connected nets has same name

Hierarchy connector...

Consider that connected nets have same net name among hierarchy levels.

Sheet connector...

Consider that all nets connected to components that have same part name are identical.



Components for board design (useWithLayout)

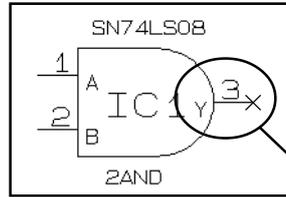
Select YES (output) or NO (no output). To omit this process, select [YES]

Property values for net output must be assigned to components to be outputted to net.



Property values vary depending on output net type. For details, see P.2-6 [Inputting data required for each net output].

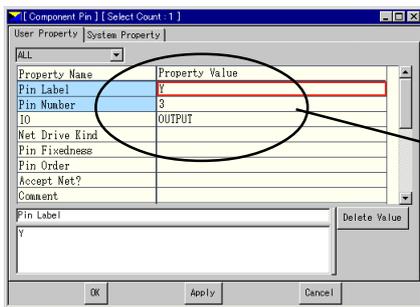
Component pin



Property values for net output must be input in component pin to be outputted to net.

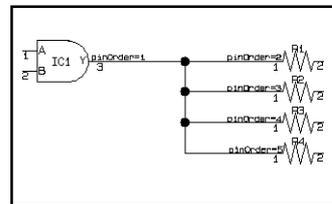
Reference Property values vary depending on output net type. For details, see P-2 [Inputting data required for each net output]

Component pin



You can output one stroke information (ONE_STROKE_NET section) by entering order of wiring in component property [Order of Wiring (order)] (As required).

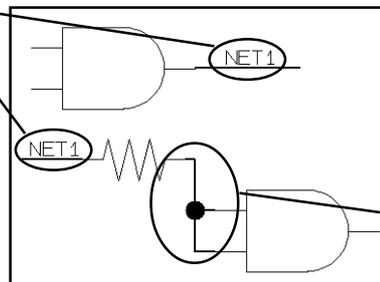
Order of Wiring.



```
ONE_STROKE_NET {
SIGN1: IC1 (3),R1(1),R2(1),R3(1),R4(1);
NetName:Reference(PinNumber),
} Reference(PinNumber), - - ;
```

Net

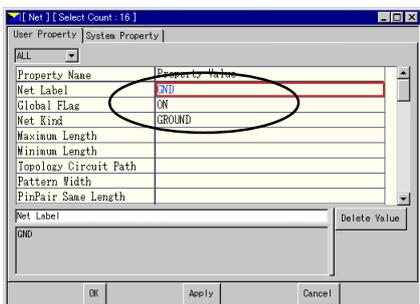
Same net



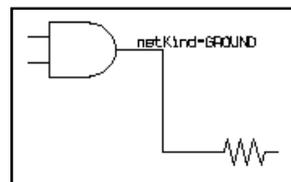
Nets connected with signal line are outputted as a series of nets.

Independent net that has same net property [net name] is also regarded as same net.

Same net



If you specify POWER or GROUND in Signal line property [net property (netKind)], that net is included in POWER or GROUND section.



```
GROUND {
GND: CN1(1),IC1(4),IC1(5),IC2(5),IC2(7);
SIGN1: IC1(3),R1(1);
}
```

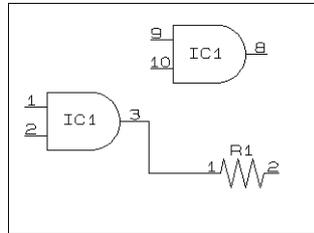
***Inputting data required for outputting each net**

For creating circuit data, required properties vary depending on output net type.

-Circuit mark net file (Without DEFINITION section) CCF

* Properties that must be input.

+ Properties that are input as required.



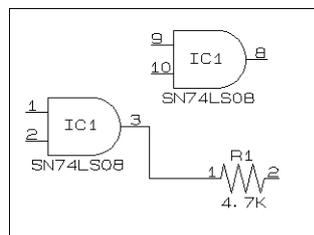
[Component properties]

*References

[Component pin properties]

*Pin number

-Circuit mark net file (With DEFINITION section) CCF



[Component properties]

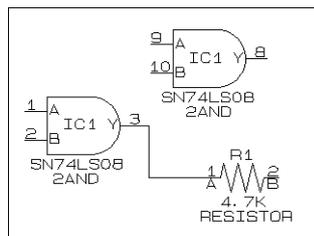
*Part name

*References

[Component pin properties]

*Pin number

-Extended circuit mark net file ECF



[Component properties]

*Part name

*References

*Function name

[Component pin properties]

*Pin number

*Pin name

[Component properties]

*Part name

+References

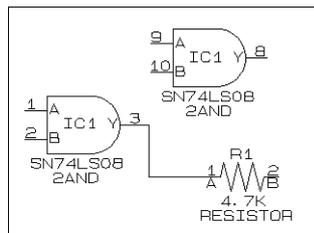
*Function name

[Component pin number]

+Pin number

*Pin name

-Gate net file GNF



If reference or pin number is omitted, these are automatically assigned to when designing board.

Correspondence with PWS properties.

System Designer		PWS
Component properties	Part name	Element name
	Reference	Circuit mark
	Function name	Symbol name
	Component ID	Symbol identifier
Component pin properties	Pin name	Terminal name
	Pin number	Pin number
Net properties	Net name	Signal name

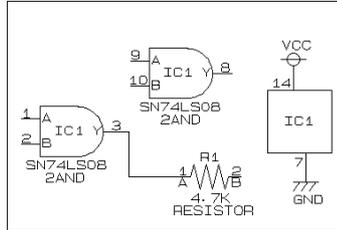


Component ID is a property automatically assigned by system (Unchangeable)
Net name is automatically assigned by system unless it is specified by users (Changeable).

***/ Provided power / Ground for IC**

Description of provided power / Ground for IC has the following 3 ways.

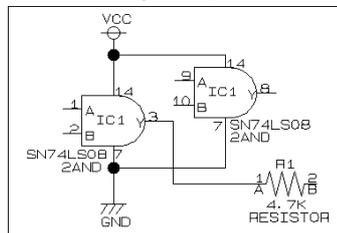
1. Description in Power BOX



Input symbols for Power BOX (**Function type: POWER BOX, Component type: Power box**) and connect to Power / Ground symbol.

Reference and pin number cannot be omitted.

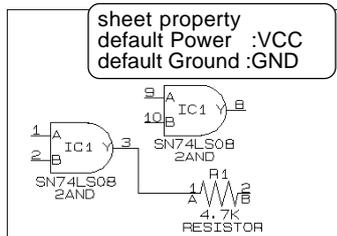
2. Connecting to symbols.



Set VCC or GND in **component pin property [IO property (io)]** for power and ground pin and connect them to Power / Ground symbol.

Reference and pin number must not be omitted.

3. Setting in default Power / Ground of sheet property.



Prepare pin set as component pin property [IO property (io)]VCC or GND within LCDB package symbol and set net name in **sheet property [Default power (defaultPower)]** and **sheet property [Default ground (defaultGround)]**.

References must not be omitted.

If you did not describe provided power / Ground for IC without using the above method, provided power / Ground for IC cannot be outputted to net file. Therefore, net file must be edited after net is outputted.

(The following description is effective for CCF or GNF with DEFINITION section)

```

DEFINITION {
:
}
:
GROUND {
  GND: CN1(1),IC1(5),IC2(5),IC2(7);
  GND::GND;
}
POWER {
  VCC: CN1(8),IC2(14);
  VCC::VCC;
}
:
}
    
```

This section is limited to net files that have correspondence with elements

Addition

Terminal name of pmaster automatically connects [GND] terminal to [Net name: GND].

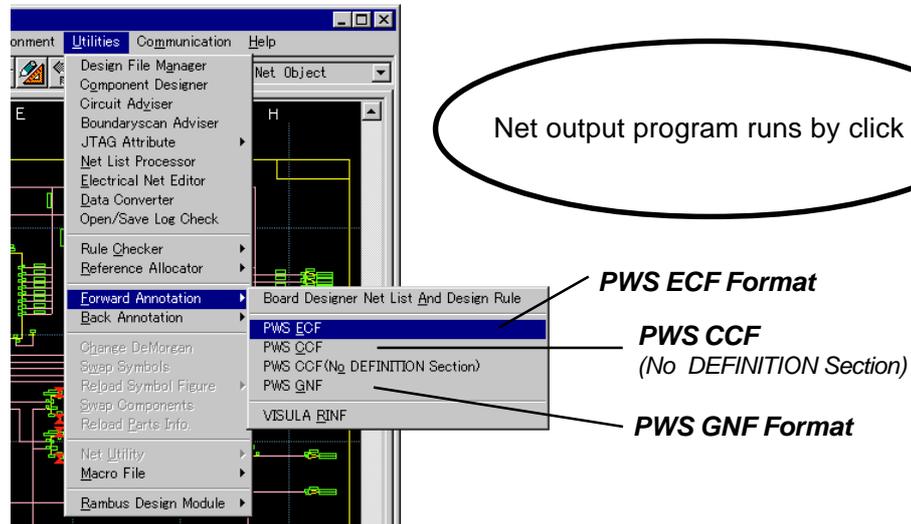
Addition

Terminal name of pmaster automatically connects [VCC] terminal to [Net name: VCC].

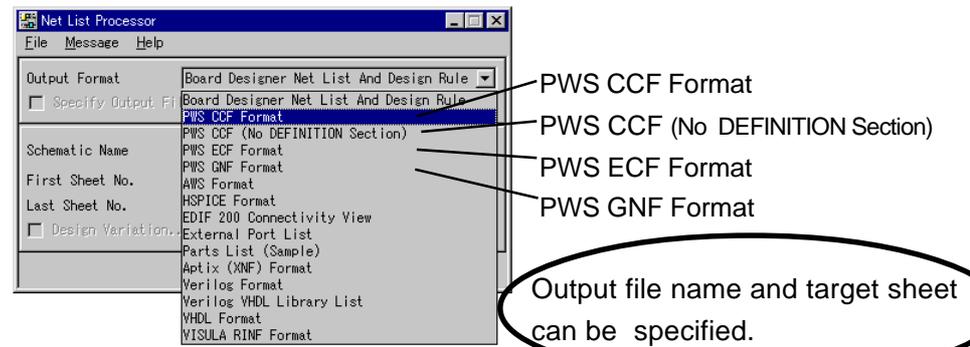
***Outputting net file**

There are 2 operation methods to output each file for PWS.

*** Menu bar / Utility -> Forward Annotation**



*** Net List Processor**



If you use **Forward Annotation** or you did not specify destination with **Net List Processor**, each file name is outputted as the following names.

Output file name	
PWS CCF Format	Circuit name. cir / ext / circuit name. ccf
PWS CCF (No DEFINITION Section)	Circuit name. cir / ext / circuit name. ccf
PWS ECF Format	Circuit name. cir / ext / circuit name. ecf
PWS GNF Format	Circuit name. cir / ext / circuit name. gnf

*Outputting Component Specific File (MSF)

In PWS, component figure is controlled by number. To get a component to be used on a board, its component number must be specified. It is available to get component figures collectively by previously creating component number list.

(Component assignment)

This component number list is referred to as "Component Specific File (MSF)".

This file can be outputted from System Designer.

/ About Component Specific File (MSF)

Component Specific File has the following description.

```
$MSF {
  /* --- CR-5000 SystemDesigner >> CR-3000 MSF ----- */
  SHAPE {
    101 : IC2      ;
    102 : IC1      ;
    103 : R1 , R2   ;
    104 : CN1      ;
    PCMACRO Number: Refrence, Refrence, - - - ;
  }
}
```



CAUTION

Component Specific File (MSF) has another 2 description methods except the above format. However, these cannot be outputted from System Designer.

The following procedure is required for outputting Component Specific File (MSF) from System Designer.

*Customizing System Designer.

Preparing environment for outputting Component Specific File (MSF).



Super user should not start System Designer for operating environment file.

1. Preparing property item.

Prepare property item [PCMAC1] for component property.

\$ZDSROOT/etc/jpn/PropSpec

```
.$Sheet {
.$Component {
  ( partName text "Part Name" ON CIRC -1)
  ( $RefTable "UserComponent")
}
#####
# User Define
#####
UserComponent{
# ex)
# (_price int "price" ON CIRC -1)
# (PCMAC1 text "PWS PCMACRO NO 1" ON CIRC -1)
}
```

← Addition.



If it has already been prepared, you do not have to add.

2. Preparing format file for outputting Component Specific File (MSF)

Create output format file named "XXX.frm" under \$ZDSROOT/etc.

Sample of format file for outputting Component Specific File (MSF) is prepared named "cr3msf.frm".

3. Editing netlist processor resource file.

\$ZDSROOT/info/jpn/dsnetprc.rsc

```
#####
# CR-5000 Netlist Formatter Resource File
# Copyright (c) 1991-2000 ZUKEN Incorporated, Japan
# ZUKEN Incorporated, R&D Division, Yokohama, Japan.
#####
format {
  ("Board Designer Net List" cr5ndf.frm CIRC)
  ("Board Designer Design Rule" cr5ruf.frm CIRC)
  ("PWS MSF Format" cr3msf.frm CIRC)
}
```

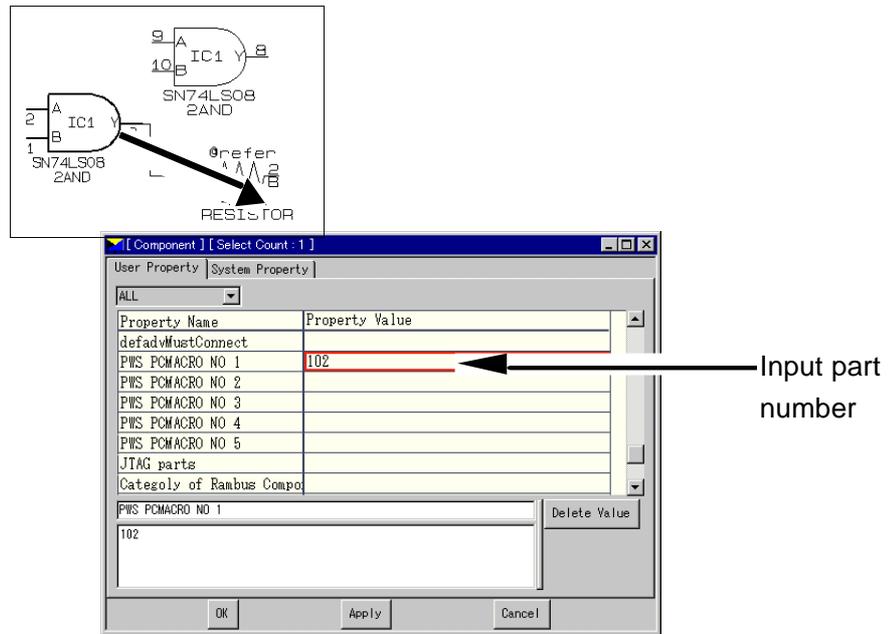
← Addition.

***Creating circuit data**

The following is procedure for outputting Component Specific File (MSF).

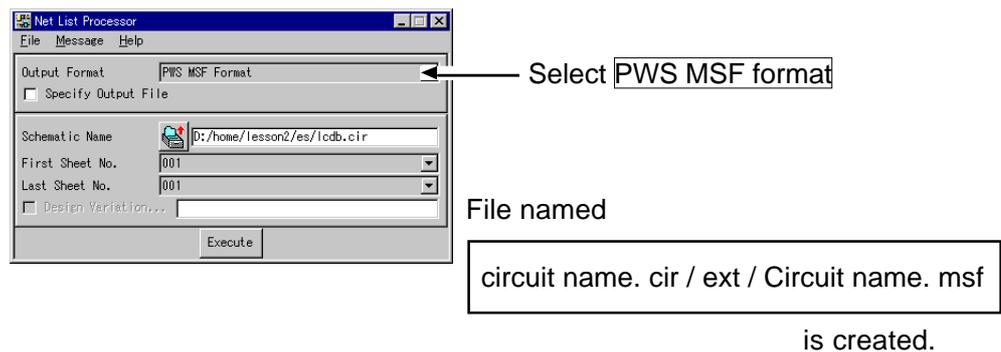
1.Inputting part number

Input PWS part number (1~16128) in component property **[PWS PCMACRO No1 (PCMAC1)]** of symbols on a circuit data.



2.Outputting Component Specific File (MSF)

Output from **Net List Processor**



***Precautions for creating a circuit data**

The following properties are used to link with PWS.

	System Designer	PWS	Text restriction
Component properties	Part name	Element name	Alphanumeric text within 20 letters
	Reference	Circuit mark	Alphanumeric text within 20 letters
	Function name	Symbol name	Alphanumeric text within 20 letters
	Component ID	Symbol identifier	Alphanumeric text within 8 letters
Component Pin	Pin name	Terminal name	Alphanumeric text within 20 letters+number
	Pin number	Pin number	Alphanumeric text within 20 letters
Net properties	Net name	Signal name	Alphanumeric text within 20 letters

In PWS, small letters are recognized as capital letters. So small and capital letters cannot be mixed to create a text. (e.g. IC1 and ic1 are recognized as identical component).

If the above properties (except component ID) are set with small letter, there is a possibility of failing to link with PWS in back annotation. So make sure to set the above properties (except component ID) with capital letter when creating a circuit data.

In addition, PWS has prohibited characters.



For details, see operation manual "For system administrator".

Data that can be transferred from System Designer to PWS are the following 3 types.

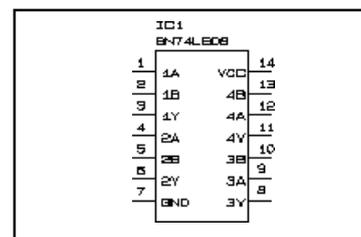
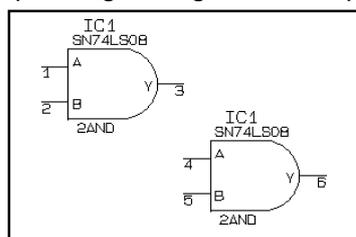
- Netlist (CCF, ECF, GNF) Connection information / one stroke information
- Component Specific File (MSF) Part number information
- Component Property Definition File (PMA) Elements information
(Shown at the back of the book)

Another all files to be used in PWS are created in PWS.

Maximum transmission line length and pattern width are properties belonging to both, however, they cannot be transferred.

- In cross-probing or back annotation, PWS links with a circuit data after netlist is outputted. Make sure not to edit a circuit data after netlit is outputted and transferred to PWS.

- Multi gates in one package symbol and one gate in one package symbol cannot be placed together with same part name on a circuit data Use only one of them depending on registration in pmaster.

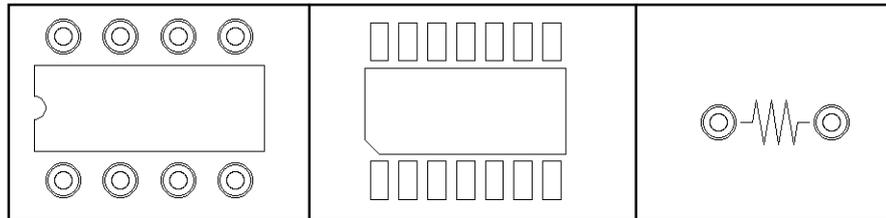


1. Registering Library

PWS has the following libraries.

*Component figure library

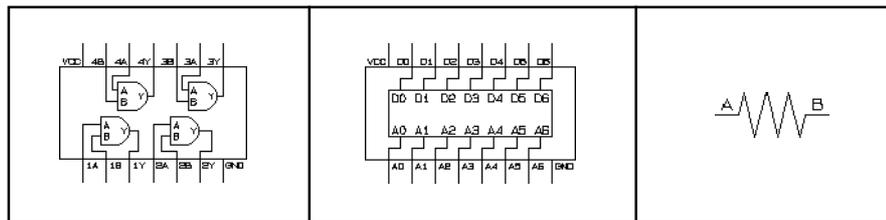
This is a library to register component figure and essential to board design.



*Component property library (pmaster)

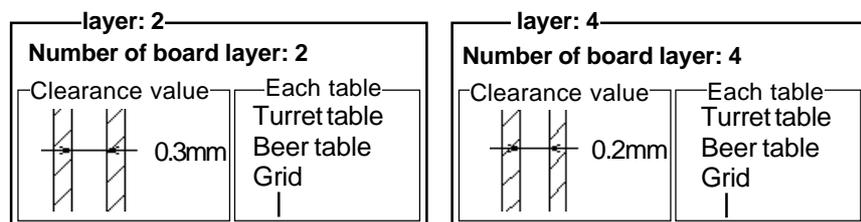
This is a library to register elements information of components and essential to the following net files.

- *Circuit mark net file (With DEFINITION) CCF
- *Extended circuit mark net file ECF
- *Gate net file GNF



*Board specification library / Wiring specification library

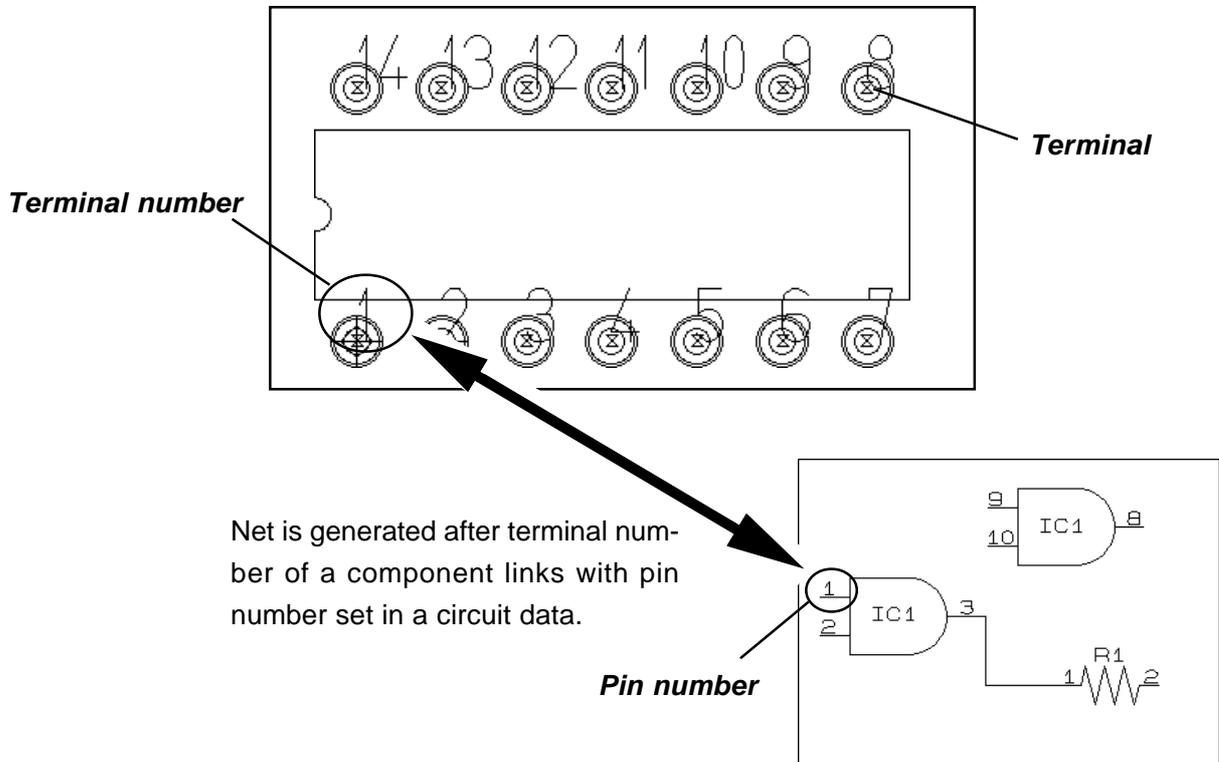
This is a library to control number of hierarchy level, clearance and each table for board design.



NOTE For board specification library and wiring specification library, there is no special precaution for using "Link between System Designer and PWS".

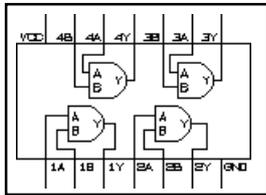
***Registering component figure**

To register component figure, set terminal in terminal part.



***Registering component properties (pmaster)**

Defining component element information.



Elements information is referred to by each program after being described in component property definition file (PMA) and registered in pmaster by using elements information definition tool. The following PMA file is a file in which pmaster information is set as ASCII and created with the elements information definition tool or

vi.

```

$PMA {
  NAME SN74LS08 : MODULE : ELSE : 1 : 4 : 14 ;
  PCMAC_NO 101 : 201 : : : ;
  SYMBOL {
    AND2 : 1, 2, 3, 4 : A, B, Y : A=B ;
  }
  PIN {
    1 : 1A : 1 : A ;
    2 : 1B : 1 : B ;
    3 : 1Y : 1 : Y ;
    4 : 2A : 2 : A ;
    :
    7 : GND : GROUND : GND ;
    :
  }
  CURRENT 40.0 ;
  IO_CURRENT {
    AND2 : A(I) : 0.02:-0.4 ;
    AND2 : B(I) : 0.02:-0.4 ;
    AND2 : Y(O) : : 0.02:-0.4 ;
  }
  USER_DEFINITION {
    1 : "ZUKEN" ; /* MAKER */
  }
}
    
```

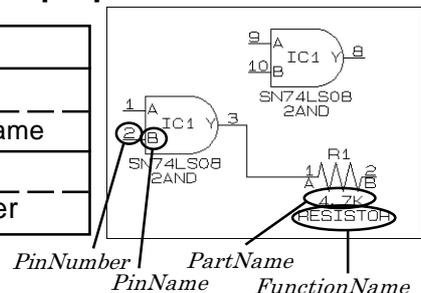
File declaration
 NAME section
 PCMAC_NO section
 (This can be omitted)
 SYMBOL section
 PIN section
 CURRENT section
 (This can be omitted)
 IO_CURRENT section
 (This can be omitted)
 USER_DEFINITION section
 (This can be omitted)

For gate number, specify as follows.
 Power terminal: POWER
 Ground terminal: GROUND
 Unused terminal: NOCONNECT

/* - */ comment

Correspondence with System Designer properties

PWS	System Designer	
device name	Component	PartName
symbol name	Property	
terminal name	Component	PinName
pin number	Pin Property	PinNumber



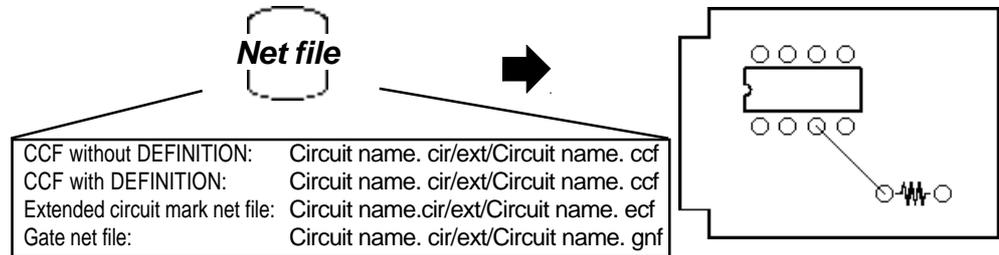
Program to convert LCDB interactively between System Designer and PWS element information library (Pmaster) is provided for consistency with System Designer.



For details of conversion program, see the back of the book.

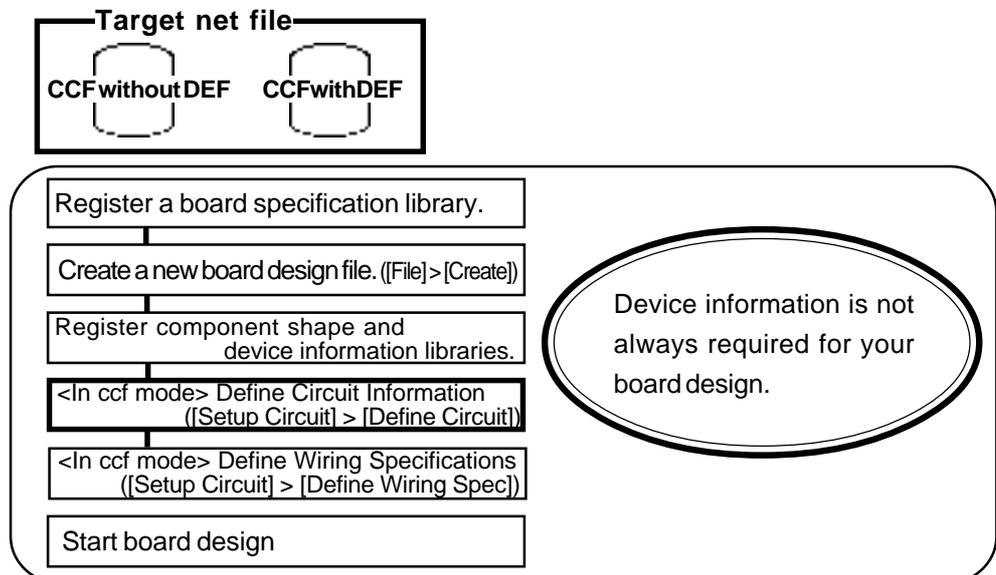
2. Creating Board

Creating board based on net file outputted from System Designer. File name is specified as follows unless you specified it.

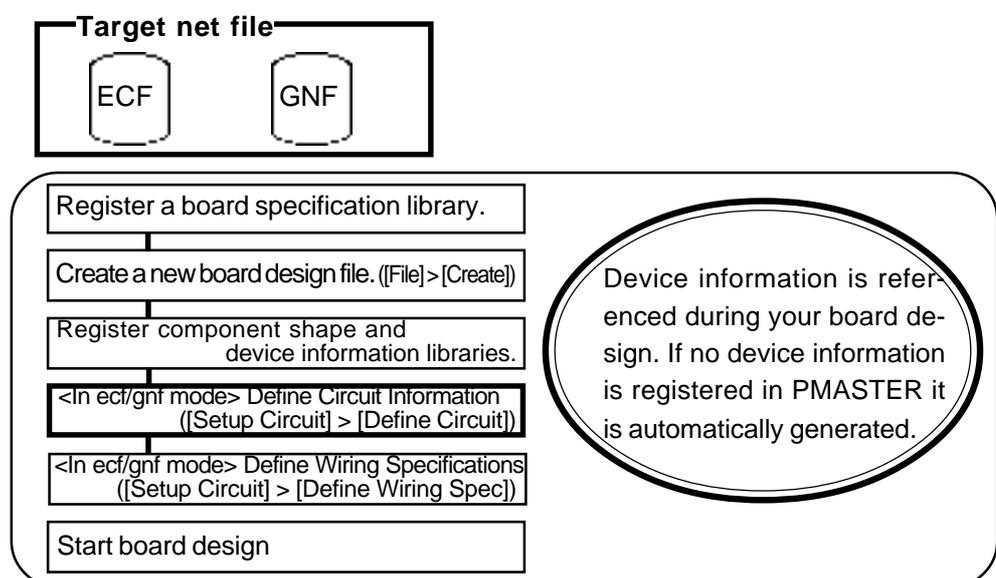


Tools to load connection information vary depending on net file type prepared for System Designer.

*Utilizing ccf operation / circuit information setting.

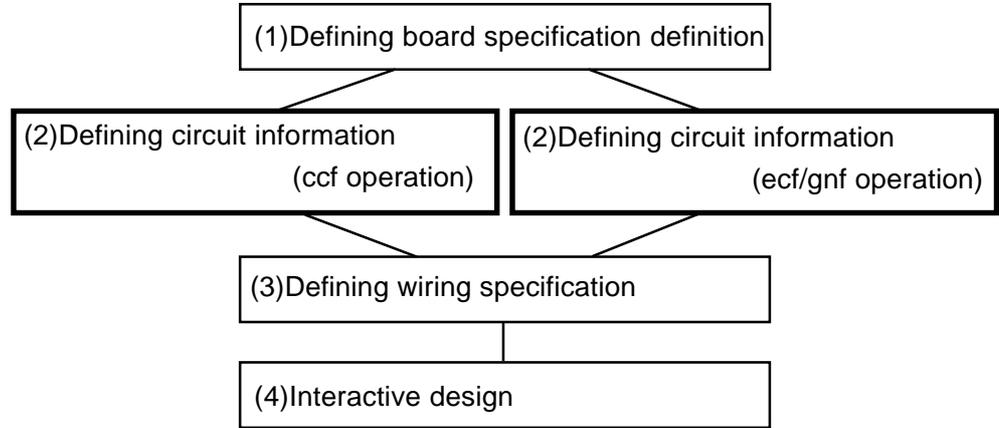


*Utilizing ecf/gnf operation / circuit information setting



***Creating board file**

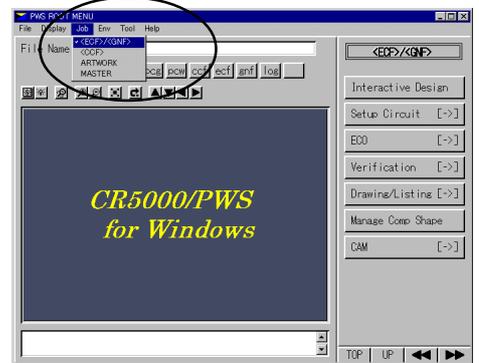
Tools used for defining circuit information vary depending on net type to be loaded.



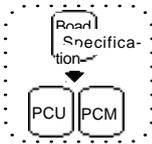
The following page describes procedure for executing each tool. Make sure that circuit information definition tools vary depending on net file type prepared for System Designer.

Startup button can be customized in PWS root menu. It is convenient to customize start up button previously because startup tools vary depending on net file type you prepared

When installation has just completed, you can start up tools according to net file type by switching between CCF operation and ECF/GNF operation in Operation of the menu bar.

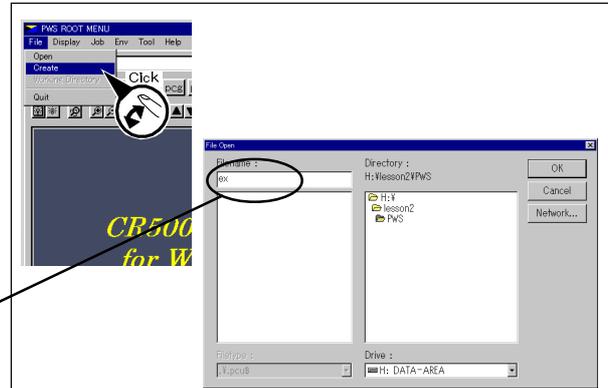


(1) Defining board specification



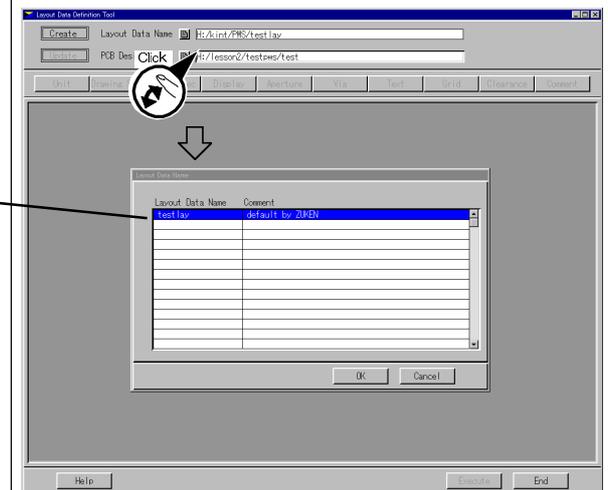
Creating board file (PCU) and component library (PCM) based on general board specification registered in board specification library.

1. In PWS root menu, click **Create** form **File** on menu bar.



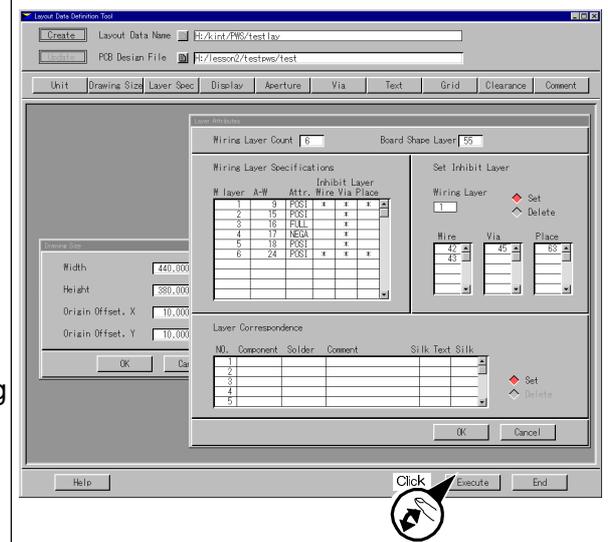
2. Enter file name from keyboard.
It is recommended that your board file name should be created with same file path name under same directory as prepared net file.

3. Select board specification name from list dialog.

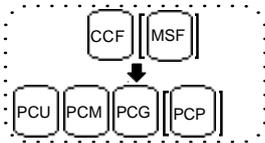


To set differently from specified board specification, click each setting button (e.g. flame size or hierarchy property).

4. Click **Execute** after checking each board specification.



(2) Defining circuit information / ccf operation

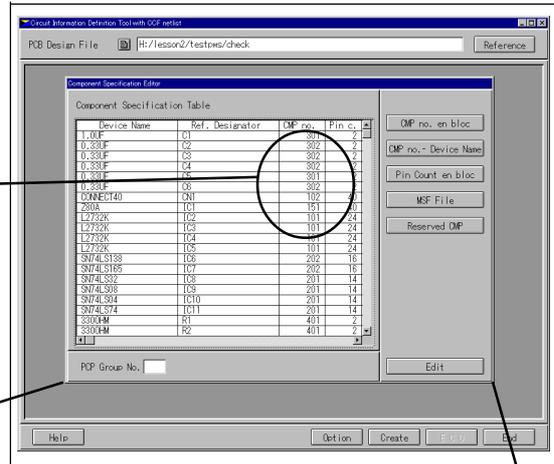


Creating gate symbol file (PCG) and components property file (PCP) based on net file (CCF). (If you created these files based on CCF file without DEFINITION, component property file (PCP) cannot be created)

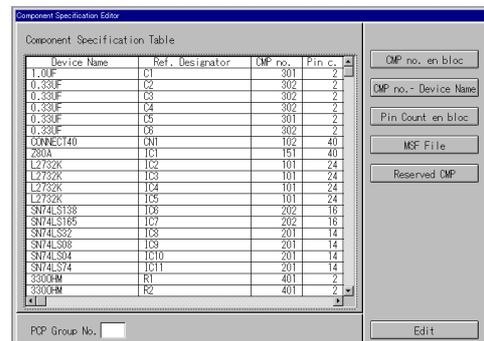
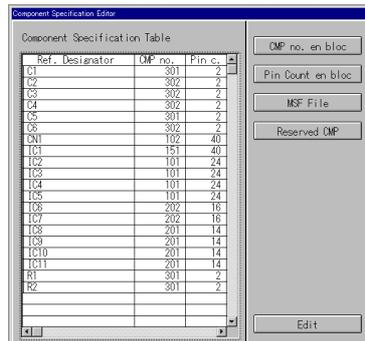
1. Click **Setup Circuit** - **Define Circuit.**

Specifying component number.

Not only loading connection information, but also assigning component figure at the same time.



Dialogs to be displayed vary depending on CCF net type to be loaded.
CCF without DEFINITION **CCF with DEFINITION**

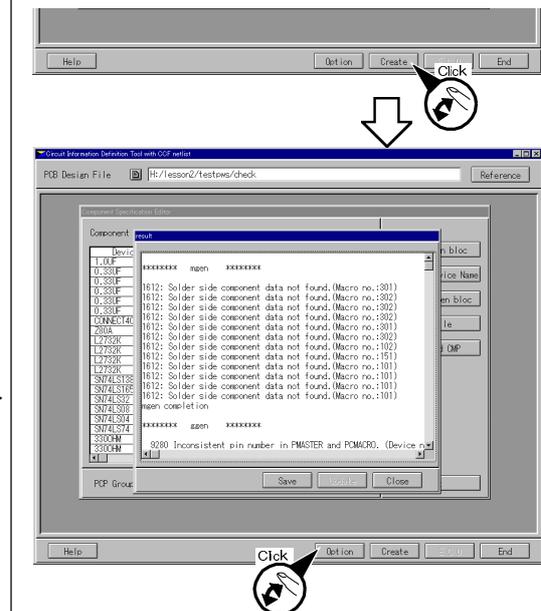


2. Click **Create**.



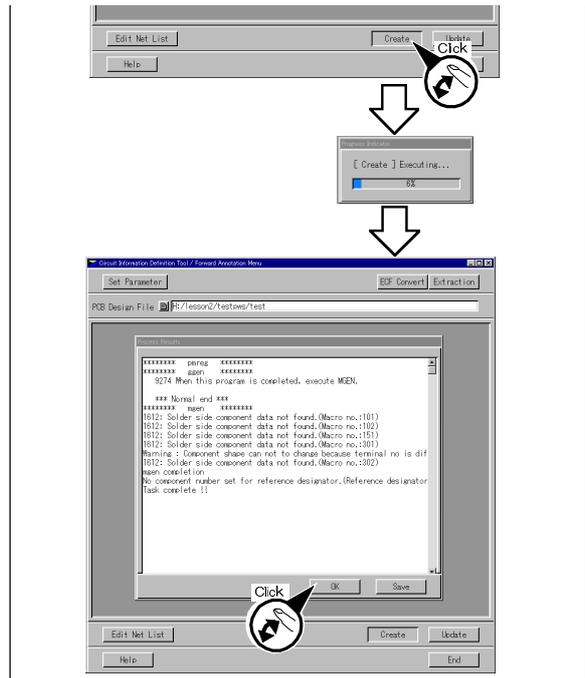
Processing results are displayed.

3. Make sure if there is no error or warning message and click **Option**.

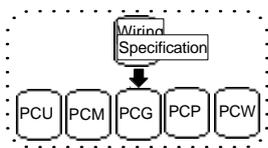


4. Click **Create**

5. Confirm if there is no error or warning message and click **OK**.



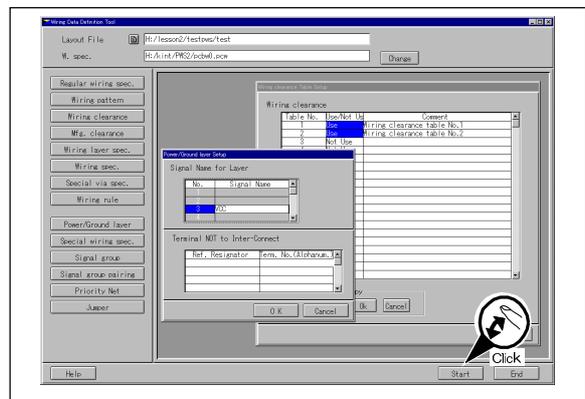
(3) Defining wiring specification



Creating wiring file (PCW) based on wiring specification.

1. Click **Define Wiring Spec.**

2. Defining wiring specification and click **Start**.



(4) Interactive design

Placing and wiring components with referring to unconnected net.

1. Starting up **Interactive Design.**

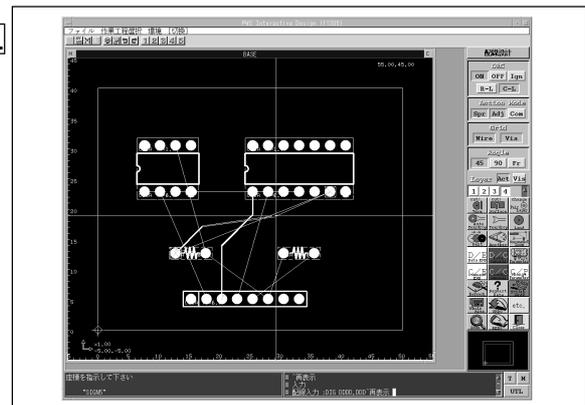
2. Inputting board outline



Placing components



Inputting wire



***Precautions for designing board**

The following properties are used to link with System Designer. (Text restriction is for PWS only and not applied to System Designer).

	System Designer	PWS	Text restriction
Symbol sheet properties	Part name	Element name	Alphanumeric text within 20 letters
	Reference	Circuit mark	Alphanumeric text within 20 letters
	Function name	Symbol name	Alphanumeric text within 20 letters
	Component ID	Symbol identifier	Alphanumeric text within 8 letters
Symbol pin properties	Pin name	Terminal name	Alphanumeric text within 20 letters
	Pin number	Pin number	Alphanumeric text within 20 letters
Net properties	Net name	Signal name	Alphanumeric text within 20 letters

Small letters on net file are recognized as capital letters.

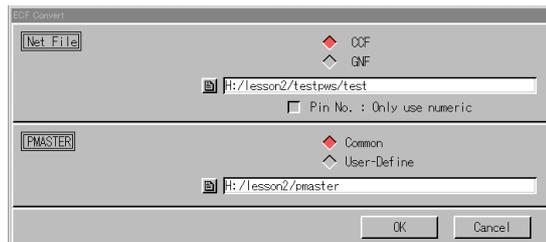
In addition, PWS has prohibited characters. Do not use the following text for the above properties.

Space " # ' () , : ; < = > { } | ~ ` TAB

It is possible to perform conversion from CCF net to ECF net by using ECF conversion in

Circuit information setting → Circuit information definition (ecf / gnf operation)

However, back annotation is not available as there is no consistency with a circuit data.

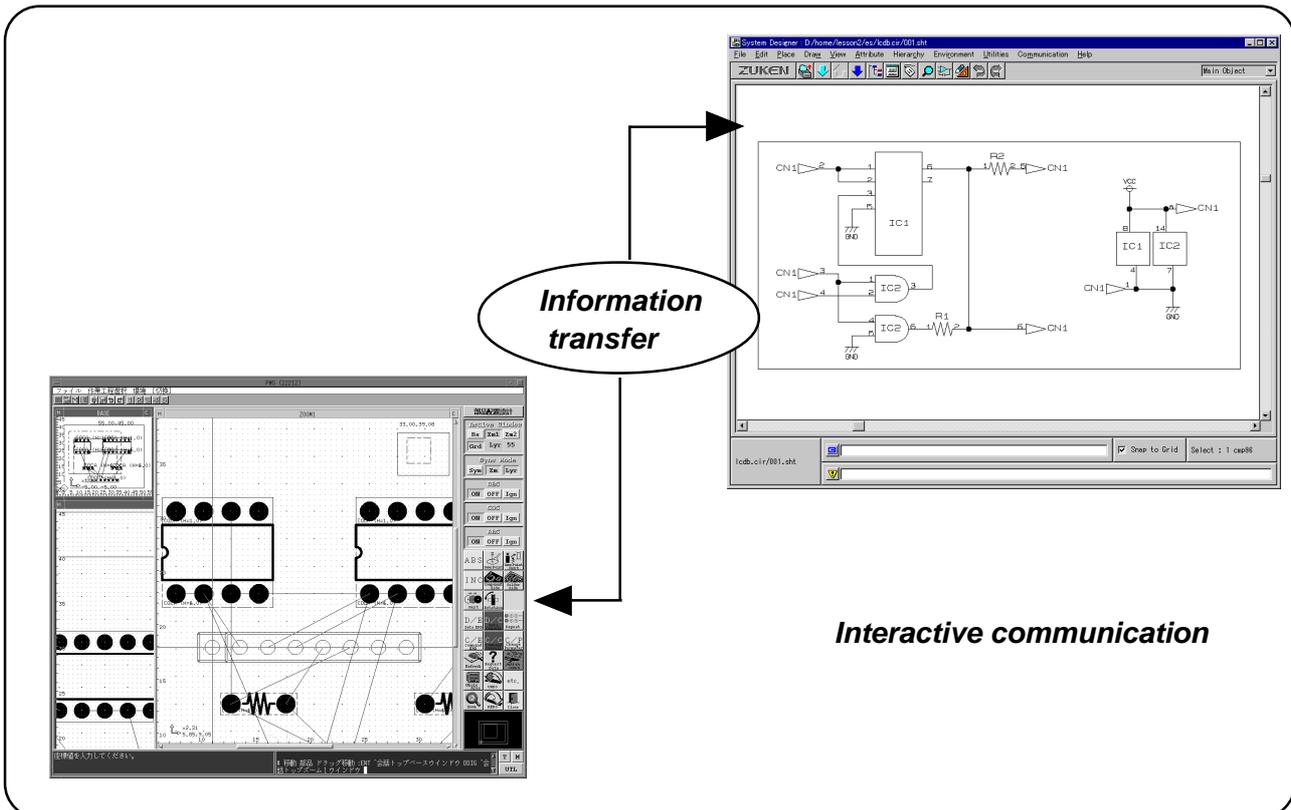


1.Utilizing Cross Probing.

*About Cross Probing

Cross Probing is a function to allow both schematic editor for System Designer and interactive design program (C3000) for PWS startup on the same display and communicate with each other.

You can design a board more effectively by checking a circuit data.



Conditions for utilizing the Cross Probing.

- PWS version Rev10.2 or higher.
- System Designer version Rev.2.132 or higher.
- Starting up program with same display and same log in user.
- Availability of data that has the following same keywords.

	System Designer	PWS
Components	References	Original circuit mark
Net	Net name	Signal name

(Whether same data or not can not be checked)

Desktop range 1280x1024 Color pallet : Hardware environment for full color (VRAM more than 4Mbyte).

Cross Probing is available with the following functions.

System Designer -> PWS

Information of specified components and nets on a circuit data is transferred to a board.

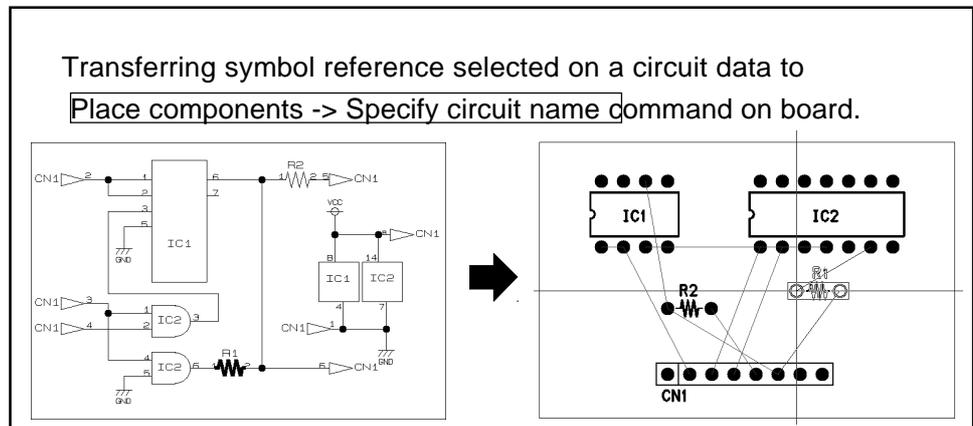
Select [Specified_Ref_Des] for the following commands.

ComponentPlace Phase: Place_Component, Away_Component, Swap, Change_Component, Copy_Component, Erase_Component, Move_Component, Auto_Zoom, Request

Select [Specify signal name] for the following commands.

Auto_Zoom-Net, Hilight_Display-Net, Display unconnected net, Check-Wire_Length, Check-Parallel_Len, Check-One_Stroke, Convdert-Wire-Surface, Lock-Delete_Lock

Example



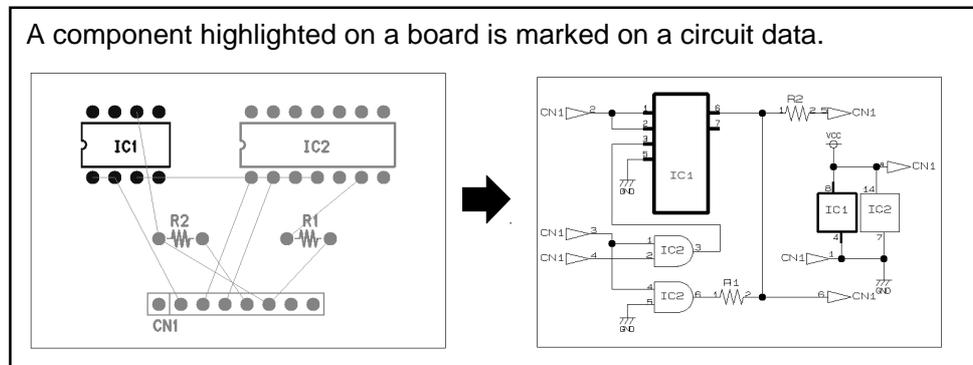
PWS -> System Designer

Specifies components and nets on a board and transfers the information to the circuit data.

Objects for [Display mark] and [Select]

Component cell / Identical potential net

Example



***Utilizing the Cross Probing between System Designer and PWS**

The following is procedure for utilizing the Cross Probing.

- 1.Enabling communication.
- 2.Using communication function.
 - A: System Designer -> PWS
 - B: PWS -> System Designer



In PWS communication function, it is possible to transfer information interactively between a board (PWS) and a circuit data (System Designer)

1.Enabling communication



Enabling communication in both PWS and System Designer. Communication function is not available if either PWS or System Designer cannot be communicated.

Setting in PWS

Specify `Comm_Schem_On` of level 0 command.

<Wiring design>

LEVEL0 (Wiring)	
Shuffle_Down	Disp_Off_Grid
Window_Refresh	Disp_On_Via_Grid
Print_Directory	Disp_Off_Via_Grid
Disp_Via_Layer	Wiring_Interval
Display_Net	Via_Interval
Disp_Net(Top)	Request_Data
Disp_Net(Bottom)	Next_Request_Data
Disp_Net(Cross)	List_Menu_ON
Disp_Net(All)	List_Menu_OFF
Display_Scale	Comm_Schem_On
Display_Coordinate	Comm_Schem_Off
Clear_Mark	Comm_Schem_Mark
Hilight_Disp_OFF	Comm_Schem_Select
Menu_ON	Update_Schem_Mark
Menu_OFF	Convert_ON
Change_Wiring_Grid	Convert_OFF
Disp_On_Grid	

<Components placement design>

LEVEL0 (Placement)	
Shuffle_Up	Menu_ON
Shuffle_Down	Menu_OFF
Window_Refresh	Main_Axis
Print_Directory	Sub_Axis
Disp_Via_Layer	Disp_On_Grid
Display_Net	Disp_Off_Grid
Disp_Net(Top)	Request_Data
Disp_Net(Bottom)	Next_Request_Data
Disp_Net(Cross)	List_Menu_ON
Disp_Net(All)	List_Menu_OFF
Display_Scale	Comm_Schem_On
Display_Coordinate	Comm_Schem_Off
Clear_Mark	Update_Schem_Mark

<Artwork design>

LEVEL0 (Art/Ut I)	
Shuffle_Up	Main_Axis
Shuffle_Down	Sub_Axis
Window_Refresh	Disp_On_Grid
Print_Directory	Disp_Off_Grid
Disp_Via_Layer	Request_Data
Display_Net	Next_Request_Data
Display_Scale	List_Menu_ON
Display_Coordinate	List_Menu_OFF
Clear_Mark	Comm_Schem_On
Menu_ON	Comm_Schem_Off
Menu_OFF	

Comms This is displayed when communication in ON.

Since Communication function is shared by each design phase, modified design phase need not be reset.

CAUTION In Component placement and Placement with examination, "Instruct circuit data" command included in popup menu is a command to link with CR-3000 / SWS. So it cannot be available in System Designer.

Setting in System Designer

Turn Communication with layout ON from `Communication` on menu bar.

ON and **OFF** can be switched.

2.Utilizing communication function

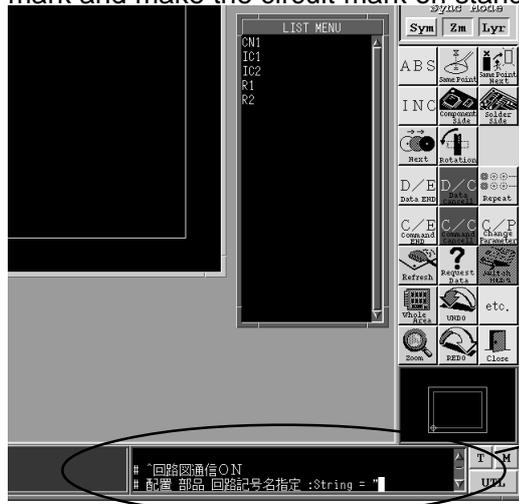
A: System Designe -> PWS

In PWS interactive design program, when executing commands to operate selected circuit mark or signal name, you can specify symbols or nets on a circuit data.

 Example

Components placement using the Cross Probing.

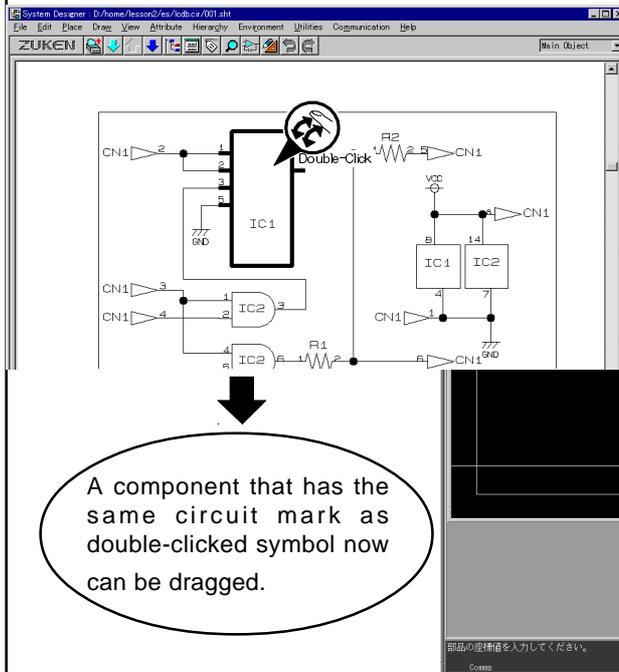
1.In PWS, execute components placement command by specifying circuit mark and make the circuit mark on standby for input.



From popup menu, select
Place component ->
Specify circuit mark ->
Input data

Make this in condition of String ="

2.In System Designer, double-click a symbol to correspond with a component to be placed on a board.



A component that has the same circuit mark as double-clicked symbol now can be dragged.

 NOTE

It is also available to execute by selecting Communication -> Transfer selected status from menu bar of System Designer while double-clicking or selecting the symbol.

A: PWS -> System Designe

Communication from PWS to System Designer is available in wiring design phase only.

 Example

Indicating mark for symbols using the Cross Probing

1.In PWS, perform setting to return [Display mark] to a circuit data

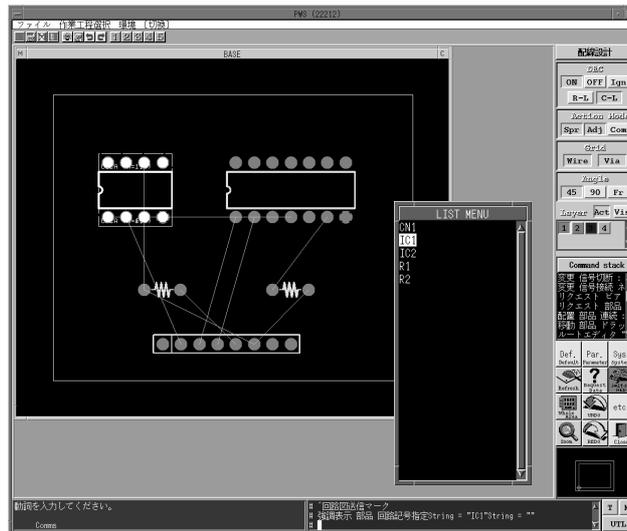
LEVEL0 (Wiring)	
Shuffle_Down	Disp_Off_Grid
Window_Refresh	Disp_On_Via_Grid
Print_Directory	Disp_Off_Via_Grid
Disp_Via_Layer	Wiring_Interval
Display_Net	Via_Interval
Disp_Net(Top)	Request_Data
Disp_Net(Bottom)	Next_Request_Data
Disp_Net(Cross)	List_Menu_ON
Disp_Net(All)	List_Menu_OFF
Display_Scale	Comm_Schem_On
Display_Coordinate	Comm_Schem_Off
Clear_Mark	Comm_Schem_Mark
Highlight_Disp_Off	Comm_Schem_Select
Menu_ON	Update_Schem_Mark
Menu_OFF	Convert_ON
Change_Wiring_Grid	Convert_OFF
Disp_On_Grid	

Select **Comm_Schem_Mark** from level0 command in wiring design.

The following 2 conditions can be return to System Designer.

Display mark
Select

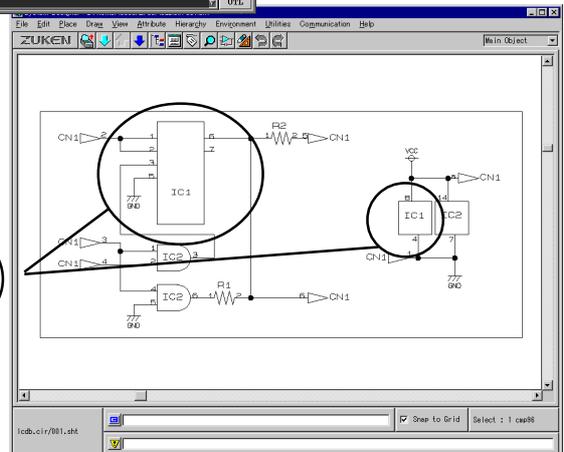
2.In PWS, highlight a component.



Select Highlight ->
Component ->
Specify circuit mark name
-> IC1
(Select from list)



A symbol that has the same circuit mark as a highlighted component is marked.



 Example

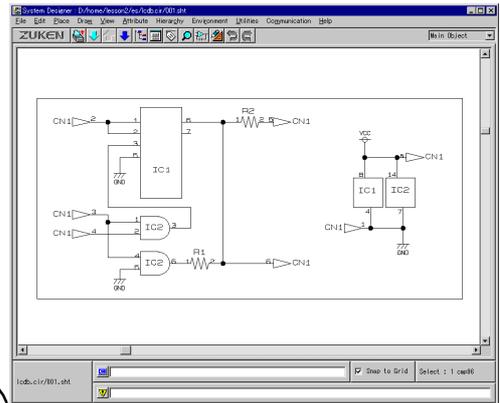
Auto mark display for unconnected net

Unconnected nets on a board are marked in System Designer. In this function, mark display changes in real time responding to wire input or delete. Mark display is also available for component placement depending on whether it is placed or not

1.In PWS, set auto mark display function.

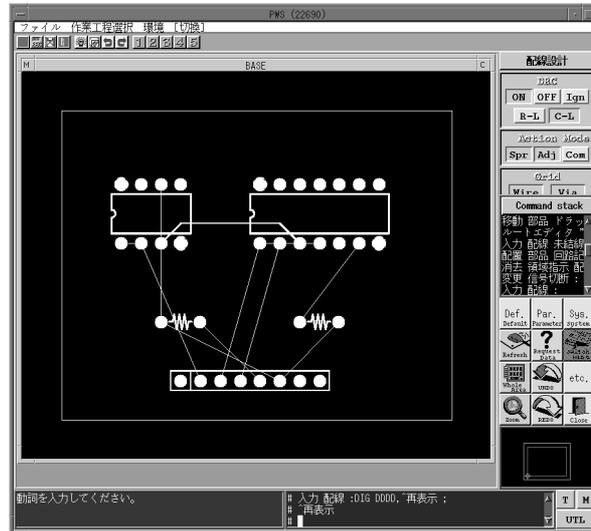
Select **Update_Shem_Mark** from level 0 command in wiring design or component placement design.

LEVEL0 (Wiring)	
Shuffle_Down	Disp_Off_Grid
Window_Refresh	Disp_On_Via_Grid
Print_Directory	Disp_Off_Via_Grid
Disp_Via_Layer	Wirng_Interval
Display_Net	Via_Interval
Disp_Net(Top)	Request_Data
Disp_Net(Bottom)	Next_Request_Data
Disp_Net(Cross)	List_Menu_ON
Disp_Net(All)	List_Menu_OFF
Display_Scale	Comm_Schem_On
Display_Coordinate	Comm_Schem_Off
Clear_Mark	Comm_Schem_Mark
Hi_Light_Disp_Off	Comm_Schem_Select
Menu_ON	Update_Schem_Mark
Menu_OFF	Convert_ON
Change_Wiring_Grid	Convert_OFF
Disp_On_Grid	



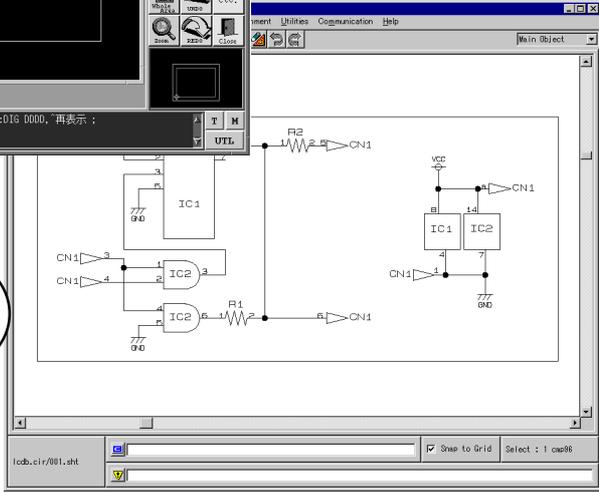
A net that corresponds to unconnected signal name is marked.

2.In PWS, wire unconnected net.



Select **Input -> Wiring -> Date -> Input -> P1 P2 - Pn**
(Specify coordinates)
-> **Date end** from popup menu.

Mark display for a net that corresponds to already wired signal name is cleared.

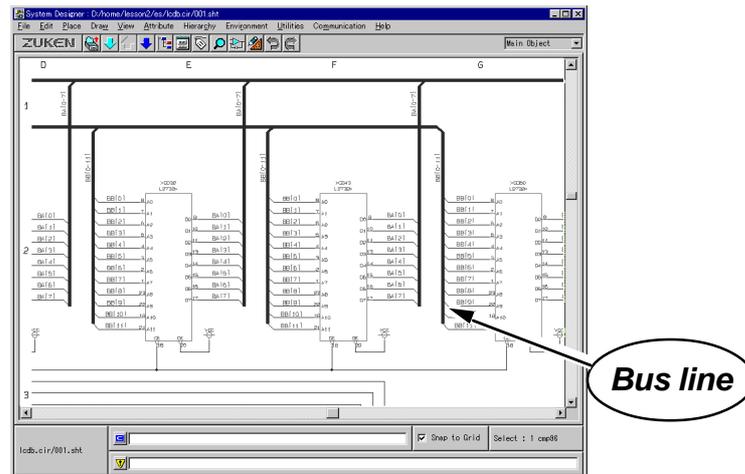


***Caution / Restricted matter**

The following data are not supported for communication with PWS.

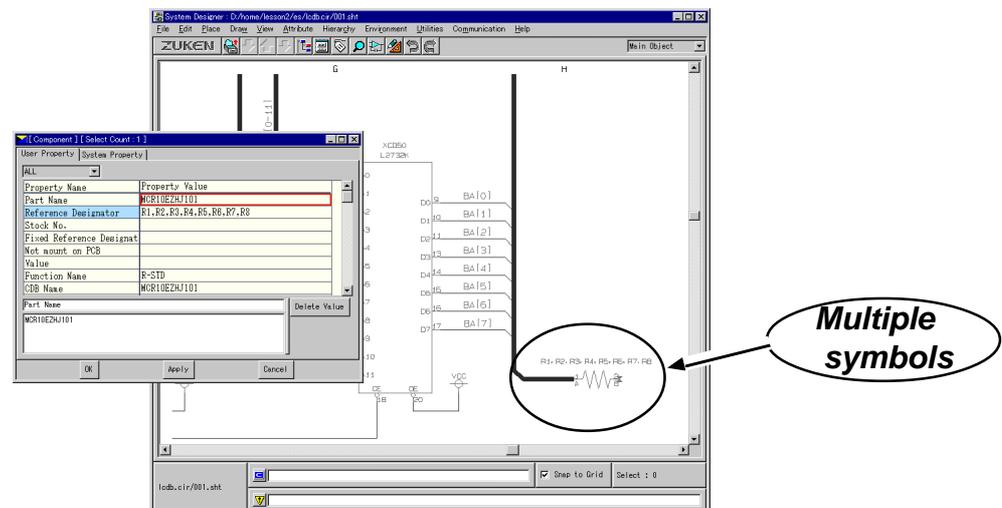
Bus line

Bus line is not supported. However, signal line connected to bus line is supported for mark display / selection.



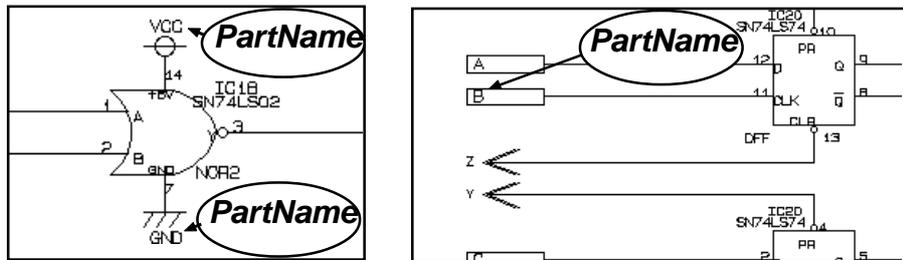
Multiple symbols

A component that stands for multiple symbols is not supported.



Circuit data in which net name is added as part name

As the following charts show, data in which power / ground net name is assigned to a symbol as part name, or data in which net name is assigned to sheet connector as part name but not assigned to signal name itself is out of target.



Objects that do not exist on both data, such as wiring jumper.

Reference name (original circuit mark) and net name (signal net name) should be keyword for communication, so data in which these names are not input is out of target.

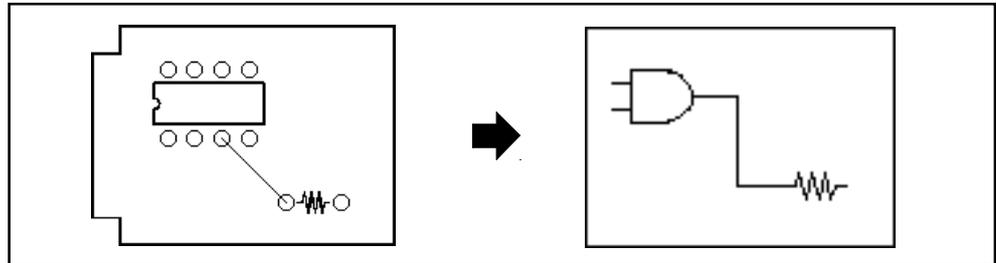
In addition, pin number, part name (element name) and so on are not checked here.

Error or warning message is not outputted for data not existed in SD.

2.Executing Back Annotation

*About back annotation

If circuit information is changed as a result of gate exchange, etc in PWS, modified information can be returned to a circuit data in System Designer.



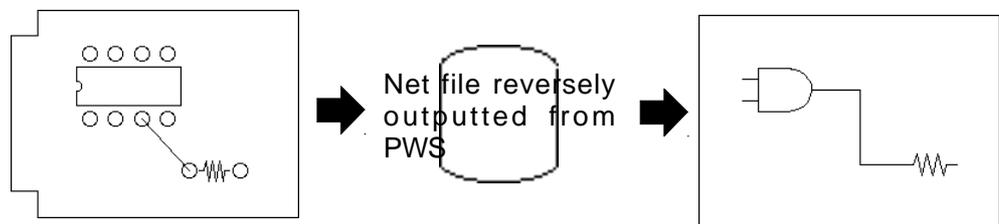
Back annotation is available only when board design is performed by using the following net files.

- Extended circuit mark net file ECF
- Gate net file GNF



CAUTION Back annotation is not available when you create a board by converting CCF into ECF.

Information of back annotation is transferred via net reversely outputted from PWS



Information to be back-annotated to a circuit data vary depending on reversely outputted net type

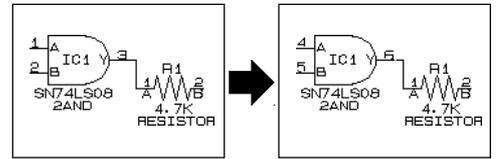
Information of back annotation	ECF	GNF
Pin/Gate exchange	Available	Available
Change of circuit mark (Reference)	Available	Available
Addition / Deletion / Change of component	Available	Not available
Addition / Deletion / Change of net	Available	Not available

When a board is created based on GNF, all information can be returned by reversely outputting ECF. (Modified information does not change).

Modified information is applied to a circuit data as follows.

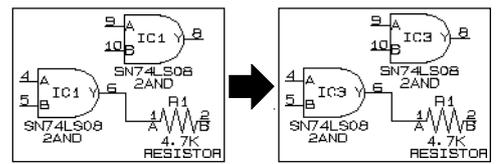
Pin/Gate exchange

When gate or pin was exchanged on a board, pin number of symbol pin is changed on a circuit data.



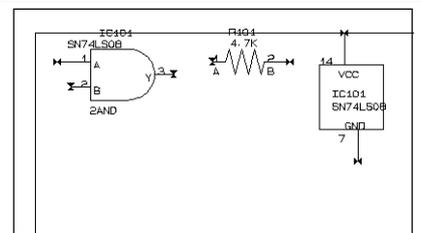
Change of circuit mark (Reference)

When circuit mark was changed on a board, modified references are applied to corresponding symbols on a circuit data.



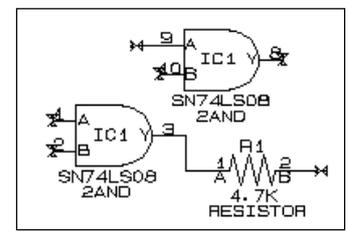
Addition of component

When connecting to undefined gate or adding a component using circuit information definition (FWD), corresponding symbol is generated on 999. sht of circuit data.



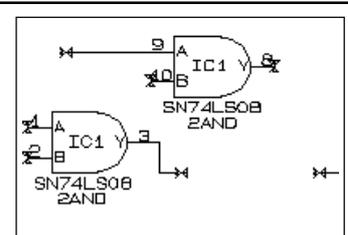
Addition of net

When connecting to undefined terminal on a board or generating new net, short signal line is generated from symbol pin on a circuit data. (Connection is not visible, however, internal connection is actually done by net name.)



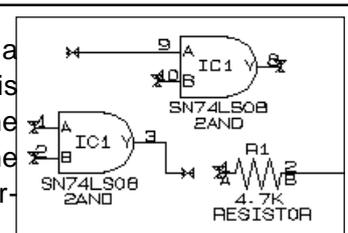
Deletion and change of components.

When a component (symbol identifier) is deleted, corresponding symbol on a circuit data is also deleted. If a symbol identifier remains, corresponding symbol on a circuit data is not deleted. When changing a component, deletion and addition are processed at the same time.



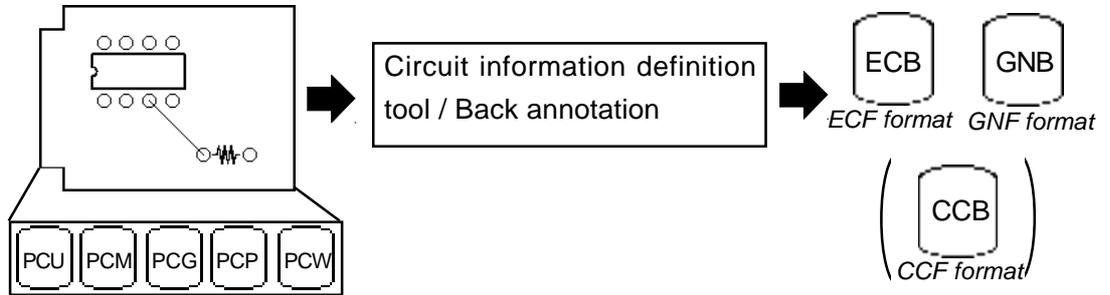
Deletion and change of nets

When changing connection or deleting net on a board, a part of net generated from symbol pin is deleted on a circuit data. When another signal line is connected as a result of connection change, the above process and signal connection are performed at the same time.



***Operations on PWS**

Output net file for back annotation from completed board file.



Target board file must have correspondence with elements (i.e. Board that contains PCP)



It is possible to reversely output net from a board in CCF format (CCB), however, CCB cannot be transferred to System Designer.

Outputted net files change each extension as follows.

ECF -> ECB
GNF -> GNB
(CCF -> CCB)

Outputted extensions are transferred to System Designer as they are.

Circuit information definition tool / Back annotation

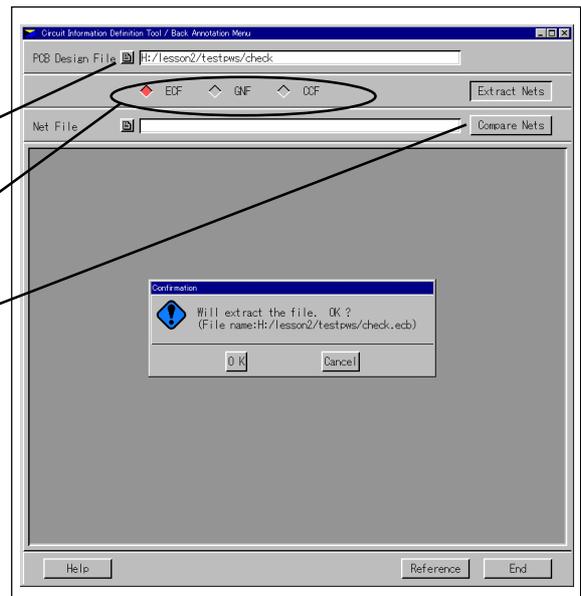
Output net file reversely from board file (PCU, PCM, PCG, PCP, PCW)

1. Click **Back Annotation**

2. Specify board file name for net output

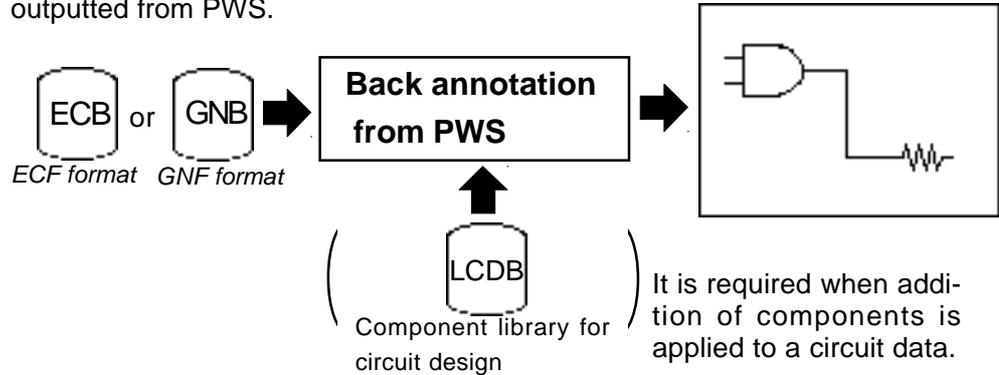
3. Select output net format

1. Click **Extract Nets**



***Operations on System Designer**

Back-annotate data to a circuit data on System Designer via net file reversely outputted from PWS.



It is required when addition of components is applied to a circuit data.

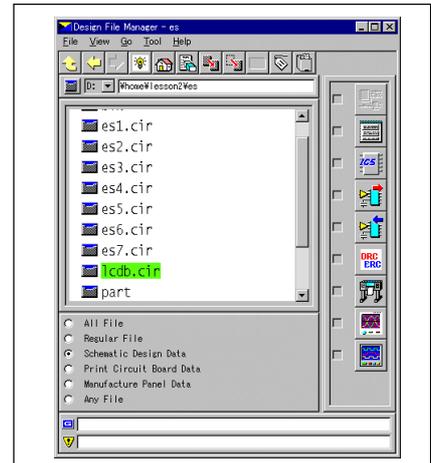
Back annotation from PWS.

Apply information of reversely outputted net file (ECB/GNB) to a circuit data.

1.Click schematic directory (~.cir) from Design File Manager.

2.Click on 

Alternatively, choose Utility (from the menu bar) > Back Annotation > PWS.

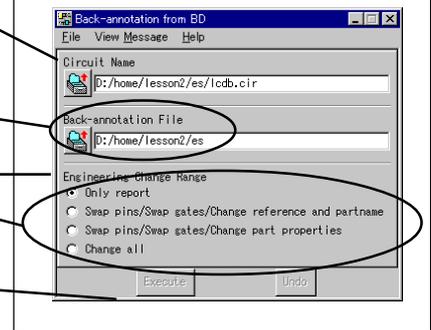


3.Specify circuit directory name to be back annotated.

4.Select reversely outputted net file type.

5.Specify reversely outputted net file name.

6.Click **Execution**



About back annotation report file

When back annotation is performed, report for modified part is created. If some modifications were not applied to a circuit data, modify them one by one with referring to the report.

Report file name: Circuit data. cir / log / ds3back. Rep

```
#####
#
#           Back-annotation Report
#
#   Schematic Name : pcbw0.cir
#
#   Date/Time : Fri Apr 06 11:17:54 2001
#
#####
#
#   Gate Swap : 0
#   Pin Swap : 0
#   Reference Change : 2
#   Parts Change : 0
#   Connection Change : 4
#   Component Addition : 0
#   Component Deletion : 2
#
#####
=====
=
=   Gate Swap/Pin Swap/Reference Change/Parts Change/Connection Change
=
=====

-----
reference: IC1
-----

Connection Change : A[1]   -> A[2]   : A12(2) : sht1.cmp90.cpn2
Connection Change : A[2]   -> A[1]   : A13(3) : sht1.cmp90.cpn3
Connection Change : A[3]   -> A[4]   : A14(4) : sht1.cmp90.cpn4
Connection Change : A[4]   -> A[3]   : A15(5) : sht1.cmp90.cpn5

-----
reference: R1
-----

Reference Change : R2      -> R1      : sht2.cmp27

-----
reference: R2
-----

Reference Change : R1      -> R2      : sht1.cmp33

=====
=
=   Component Deletion
=
=====

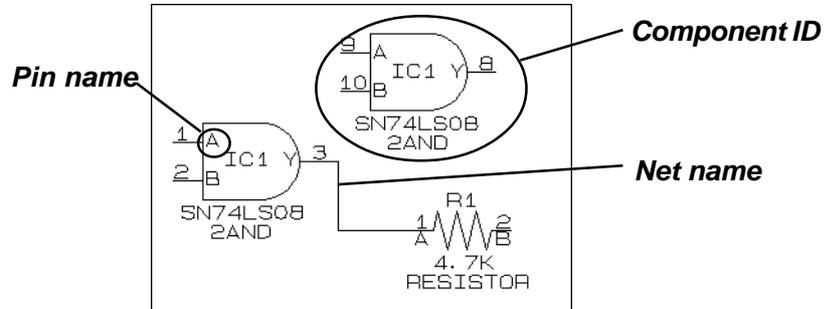
-----
reference: IC1
-----

Object ID       : sht1.cmp91
Part Name       : Z80A
Function Name    : Z80A
CDB Name        : Z80A
Block File Name :
```



*Precautions for back annotation

- * Back annotation finds out modification by making a comparison between net file outputted from PWS and one outputted from a circuit data again. The following properties can be keyword for back annotation.



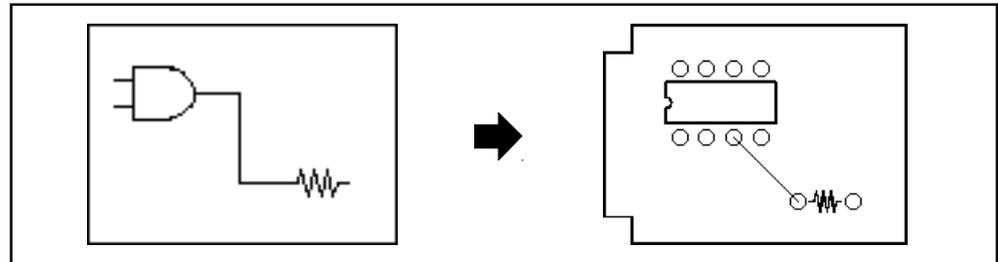
Among these properties, component ID (automatically assigned by system) is an absolute keyword. If component ID is modified by using symbol exchange command after net output, which causes error in back annotation and information cannot be returned to a circuit data. So make sure not to change component ID.

- * When a component without elements is added by using Input placement component of interactive design (C3000) in PWS, the information cannot be returned to a circuit data. So make sure of specifying element name when you add components.
- * If you described net name or reference in small letter on a circuit data, these are recognized as capital letter in PWS. As back annotation returns information to a circuit data in capital letter, there is a possibility that system misunderstands modification part, e.g. for net name, connection is regarded as change, for part name, its component is regarded as change.

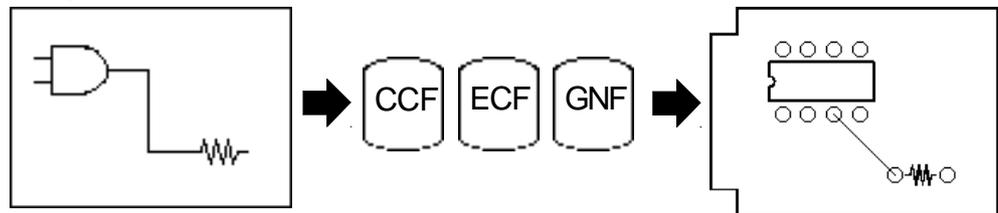
3. Modifying Design

*About design modification

If modification has been made on a circuit data after a board was created, the modification can be applied to a board by modifying design.



Modified information can be transferred via net file in the same way as board design.



Net file outputted for design modification is restricted by one used in board design.

Board Design	Design Modification
CCF	CCF
ECF	ECF, GNF
GNF	ECF, GNF

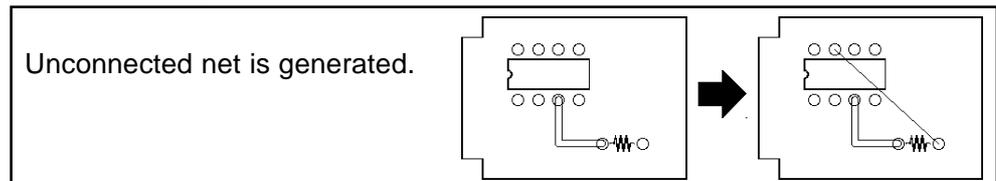
Modified information is applied to a board as follows.

***Addition of a component**

Added as a not placed component

----- Up component -----				
Comp no.	Component name	Reference desinator	Component type	Component
302		C1	DIP type	module
302		C2	DIP type	module
302		C3	DIP type	module

Addition of signal line



Deletion / Change of a component

When a component is deleted from a circuit data, it is also deleted from a board. For changing a component figure (change of part number), deletion and addition are processed at the same time and the component is regarded as a not placed component.

Deletion of signal line

A series of patten is deleted only when signal names disappear and connected terminals totally change due to circuit change.

Modification of signal line

When connected destination is changed, pattern from terminal to next composition point is deleted.



Methods to apply modified information to a circuit data vary depending on [Search Keyword] that is specified when you modify design in PWS.

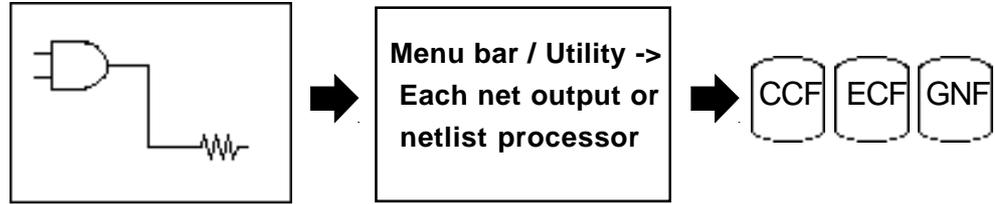
Search Keyword
Circuit mark
Signal name

Select appropriate keyword according to modified contents.

(If you used the circuit information definition (FWD) menu, specify component ID (symbol identifier) as keyword for modification.)

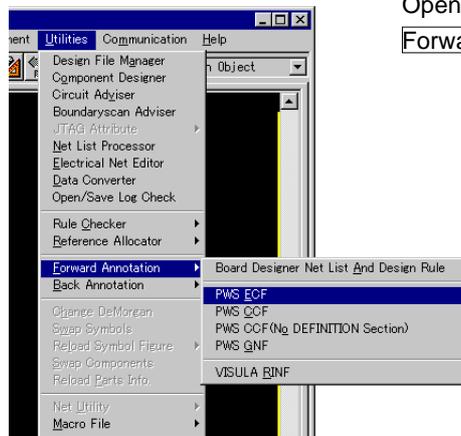
***Operations on System Designer**

Edit a circuit data and output net file again.



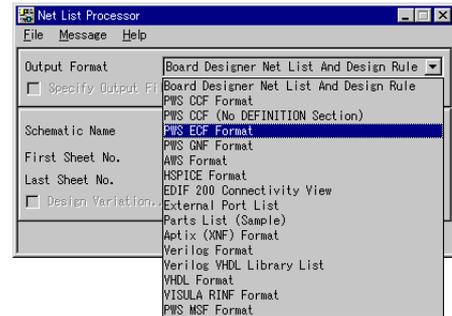
Net output

Output net again from modified circuit data.



Open a circuit data and select **Utilities** -> **Forward Annotation** -> **PWS ECF** from menu bar.

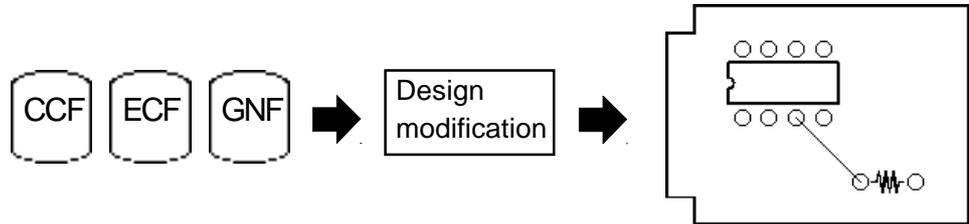
Specify net extension.



Net output is also available by selecting **Utilities** -> **Net List Processor** from menu bar in editor.

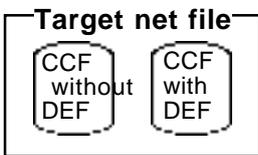
***Operations on PWS**

Apply modification to a board based on a net file outputted from a circuit data.



On PWS work, startup tools vary according to net type.

[ccf operation] Change design -> Change circuit information



When you modify data, you can specify some options in detail to apply modifications.

1. Start **Change design** -> **Change circuit information** tool in [CCF operation].

2. Specify net file in which modified information is described.

3. Click **OK**.

4. Specify part number.

Set processing mode for modification.

5. Click **Option**

Component Specification Table

Device Name	Ref. Designator	OMP no.	Pin G.
T100P	Q3	301	2
0-330P	Q2	302	2
0-330P	Q3	302	2
0-330P	Q4	302	2
0-330P	Q5	302	2
0-330P	Q6	302	2
CONNECT40	CN1	151	40
220K	R1	102	40
L2729K	L02	101	24
L2729K	L03	101	24
L2729K	L04	101	24
L2729K	L05	101	24
SN74LS128	U8	202	16
SN74LS165	U9	202	16
SN74LS22	U3	201	14
SN74LS26	U8	201	14
SN74LS24	U10	201	14
SN74LS74	U11	201	14
8203AM	R1	401	2
8203AM	R2	401	2

[ecf / gnf operation] Change design -> Change circuit information

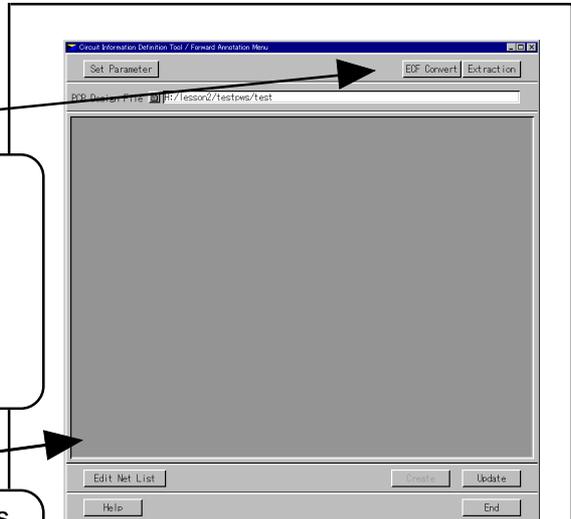
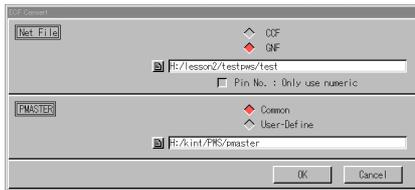
Target file



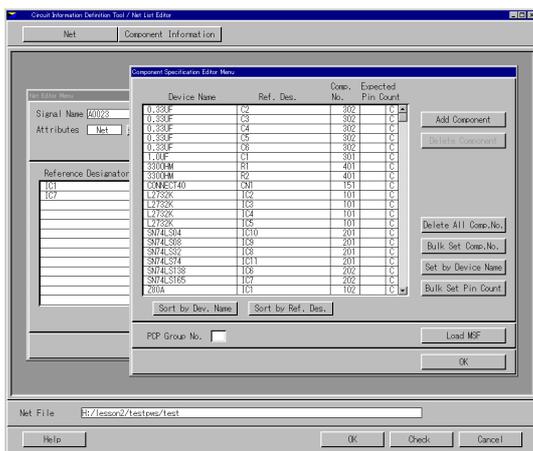
Make a modification with having correspondence with elements. It is also possible to edit net after modification.

1. Start **Change design** -> **Change circuit information** tool in [ecf / gnf operation]

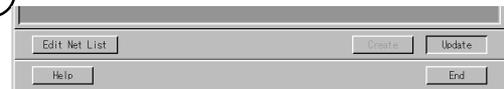
When modified net is GNF, firstly convert it to ECF file.



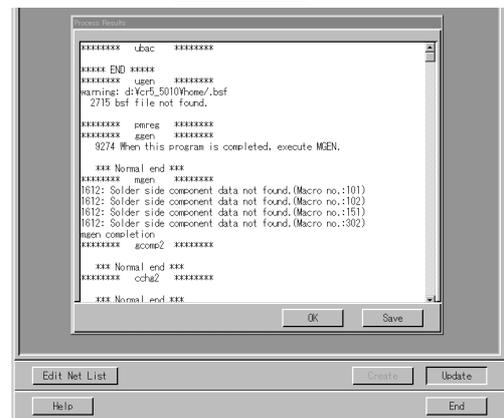
If you want to edit net information from editor, select this.



2. Click **Update**.



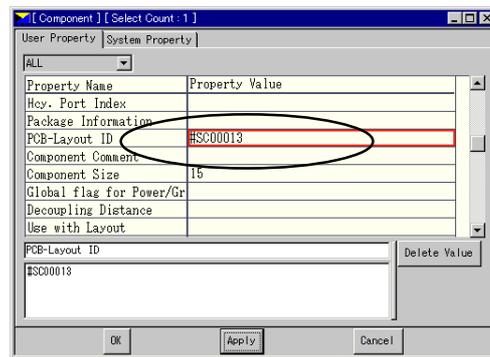
3. Check if there is no error or warning message and click **OK**.



*Precautions for modifying design

When circuit information was changed in board design side, apply modification to a circuit data by performing back annotation, then modify the circuit data.

For added symbol as a result of back annotation (component symbol added to board design), item (#SC0001) described in symbol property [PCB layout system ID] is outputted as symbol identifier and links with the component on a board.



```
$ECF {  
:  
  SYMBOL {  
:  
    1.CMP4:2AND:IC2:A(4),B(5),Y(6);  
    #SC00013:2AND:IC2:A(12),B(13),Y(11);  
:  
  }  
}
```

If one stroke information has been changed, order of one stroke on wiring data is not regarded.

If signal connected to full surface is deleted, specific processing must be required for modifying PWS design.



For details, see PWS Self-Training [Design Modification].