



Hierarchical Design

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Introduction

This <Hierarchical Design> is intended for the user to acquire the knowledge in hierarchical design performed in CR-5000/System Designer, and learn the operation for creating circuit blocks, thus implementing a smooth system operation.

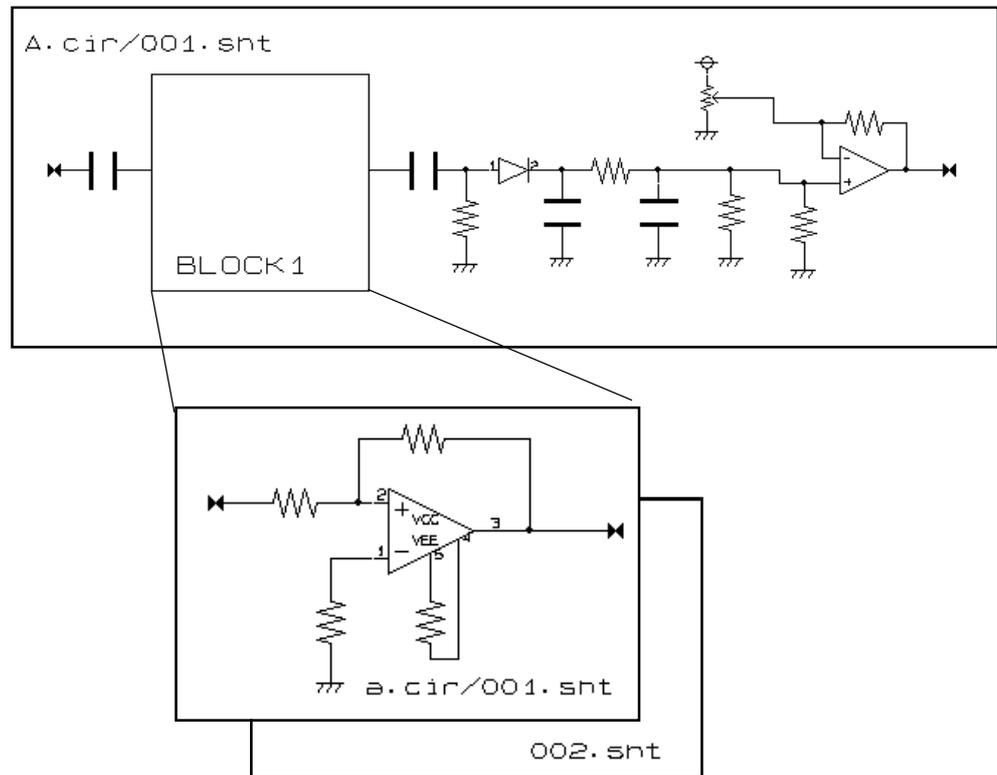
For basic operation of the System Designer, see "Operation Guide -BEGINNER-"



1. Performing Hierarchical Design

● Hierarchical Design

Circuit design is performed hierarchically by representing sections of the circuit as circuit blocks.



For example, in the above schematic, the actual circuit for the circuit block BLOCK1 input to sheet 1 of schematic directory A.cir is contained in schematic directory a.cir.

Hierarchical design can be either bottom-up or top-down design.

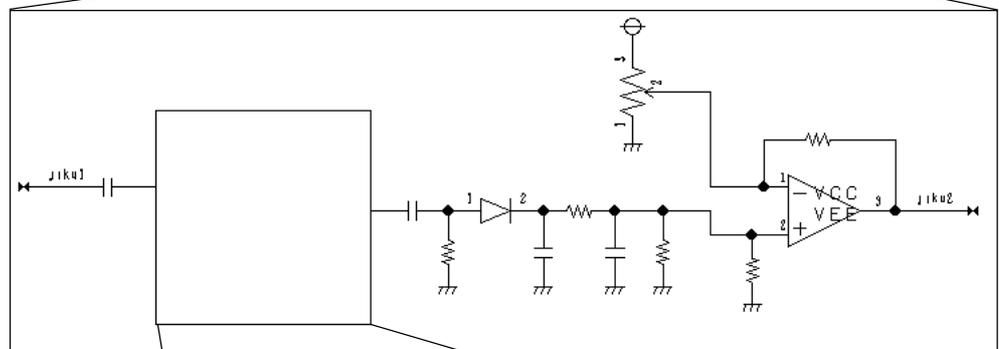
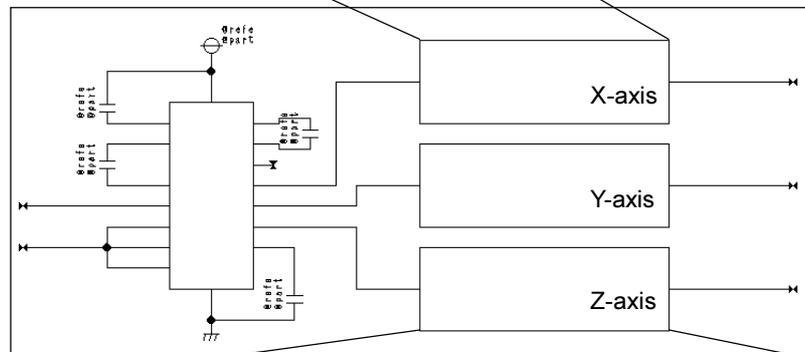
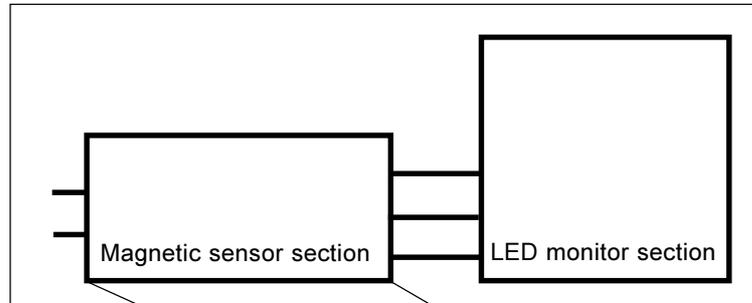
 **NOTE** For reference, see “sample3” implemented in hierarchical design.

1. Performing Hierarchical Design

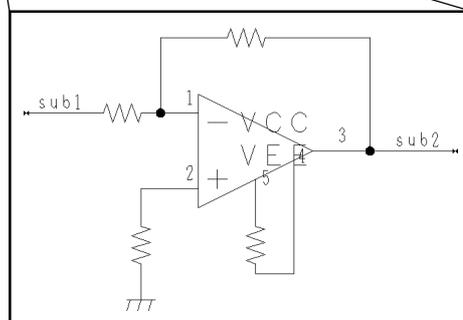
When designing a circuit to perform a specific function using top-down design, the design proceeds from the top to the bottom level by progressively splitting the circuit into smaller sections.

 **EXAMPLE** Design for a personal navigation system

Top-down design

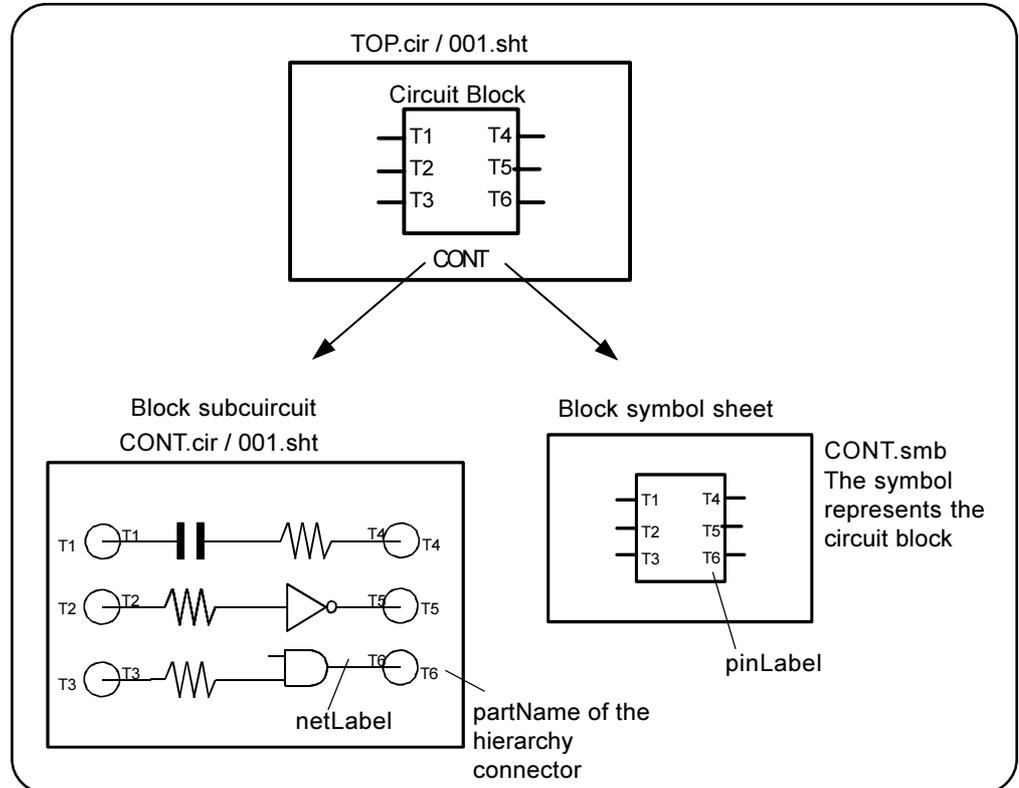


Bottom-up design



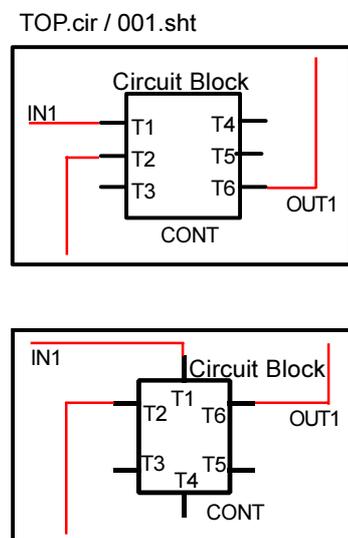
When circuits that perform specific functions can be reused either in the same circuit or in another circuit design, bottom up design for each function proceeds from the bottom to the top level.

In SystemDesigner, circuit blocks are managed using the following files and Circuitdirectory.



Connection between higher level nets and the nets within the circuit block takes effect when “pinLabel” of the block symbol and the “partName” of the hierarchical connector of the block subcircuit are of the same name. (The net Label of the net to be connected with the hierarchy connector also has the same name.)

When the part name of the hierarchy connector of the block subcircuit and the pinLabel of the block symbol have the same name as shown above, this means the connection is in place to [T1] net of the block subcircuit because net [IN1] of the higher level is connected to pin Label [T1] of the block symbol. Connection remains unchanged even if there is a different block symbol figure as shown at right.

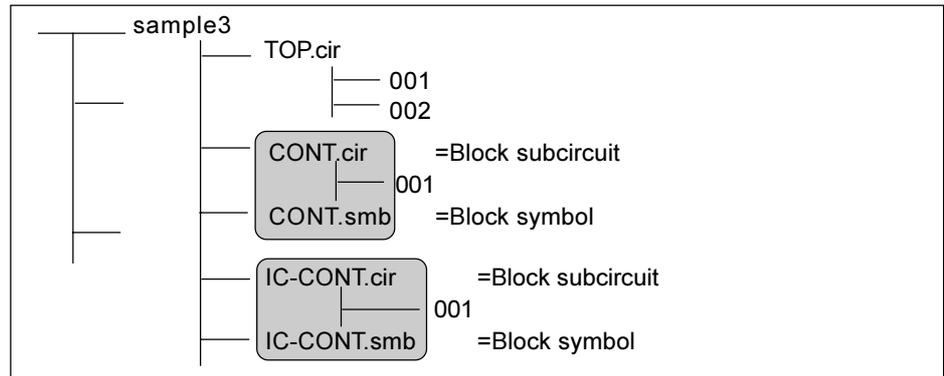




To put the circuit block into the schematic sheet, the block subcircuit and the block symbol, both of the same name, need to reside in the same directory.

Block subcircuit	xx.cir
Block symbol sheet	xx.smb

If the block subcircuit and the block symbol, both having the same name, reside under the same directory, they can be used as the circuit block. (If the circuit block is automatically created, it will be created in the same directory.)

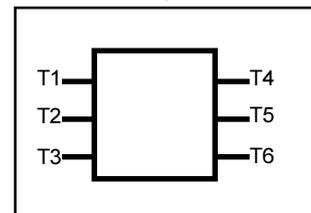
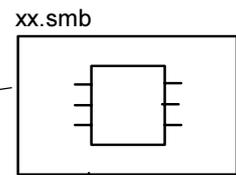
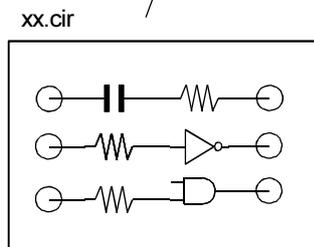


**Path to Reference*

For input of a circuit block, you need to set the directory having the block symbol and the block subcircuit to the symbol path within the Data Resource File (landata.rsc). The circuit block path will not be referenced. (The block symbol and the block subcircuit will be stored in the same directory.)

Symbol Search Path

0	current	.
1	local	./smb
2	smb1	/symbol/smb1
3	smb2	/symbol/smb2
4	blk1	/block/blk1

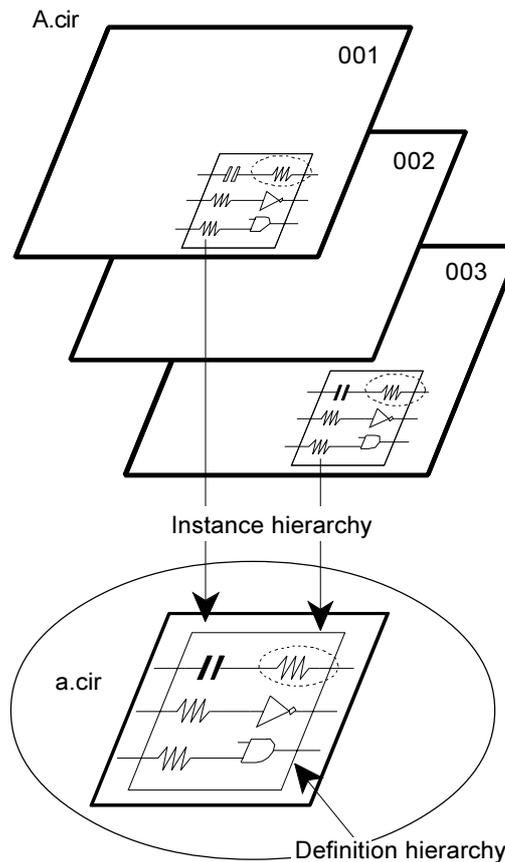


About the circuit block path:
 It will not be used for the circuit blocks created by the Rev.6.0 software.
 For circuit blocks created before Rev. 5.0, see "Circuit blocks created by the Rev.5.0 or earlier" at the end of this manual.

● Instance Hierarchy and Definition Hierarchy

When designing circuits using hierarchical design, the structure of the hierarchy is represented by the instance hierarchy and the definition hierarchy.

For example, two instances (BL1 and BL2) of a circuit block from circuit a.cir have been input to circuit A.cir, as shown in the figure below.



Circuit a.cir contains a component with the reference "R1". However, the reference information from the circuit block cannot be used on the A.cir sheet when there is more than one instance of the same circuit block (e.g. BL1 and BL2) as this results in the reference ("R1") appearing more than once.

In this case, SystemDesigner creates and stores the reference information from the circuit block in the highest level circuit directory (A.cir) based on the instance data file (instnc).

(The reference information indicates that circuit blocks BL1 and BL2 contain the R10 and R11 components, respectively.)

In this way, lower level circuit directories (a.cir) form an instance hierarchy from the viewpoint of the highest level circuit directory (A.cir).

Only instance information = property editing can be performed in the instance hierarchy.

In contrast, the circuit directories containing the circuit blocks form the definition hierarchy.

Editing of the internal circuits of circuit blocks can be performed in the definition hierarchy. Therefore, if changes to the circuit change the components or related data, this also changes the contents of the circuit blocks input to schematic directories higher in the hierarchy.

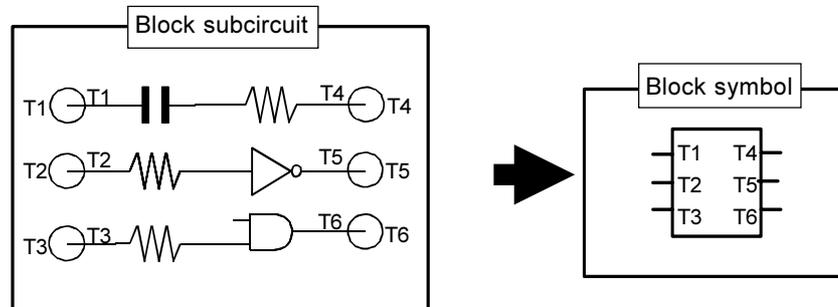
⚠ ATTENTION

When changing circuits in the definition hierarchy, note that changing the sheet size and position of net terminals in particular results in the system being unable to perform internal display of the circuit block or to expand the circuit block.

2. Creating a circuit block

● Creating a circuit block in a bottom-up manner

How to create a block symbol from the block subcircuit.



The following two methods are used to create a circuit block from the circuit being edited or from the circuit already created.

1. Automatically create the block symbol sheet from the circuit directory being edited.
2. Create the block symbol sheet with reference to the circuit directory already created.

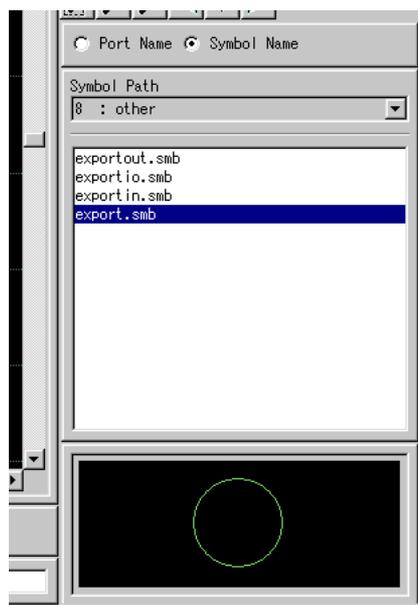
1. When automatically creating a block symbol sheet from the circuit directory being edited:

Create the block symbol after adding modification for automatic creation of block symbol in the block subcircuit.

Either of [Generate Entire Sheet's Block] or [Edit Block Symbol] will be used in the command.

EXAMPLE

1) Enter the hierarchical connector symbol into the net end point to be the pin of the block symbol.



Choose [Place] -[External Port] from the menu bar.

Switch the panel menu to [Symbol Name].

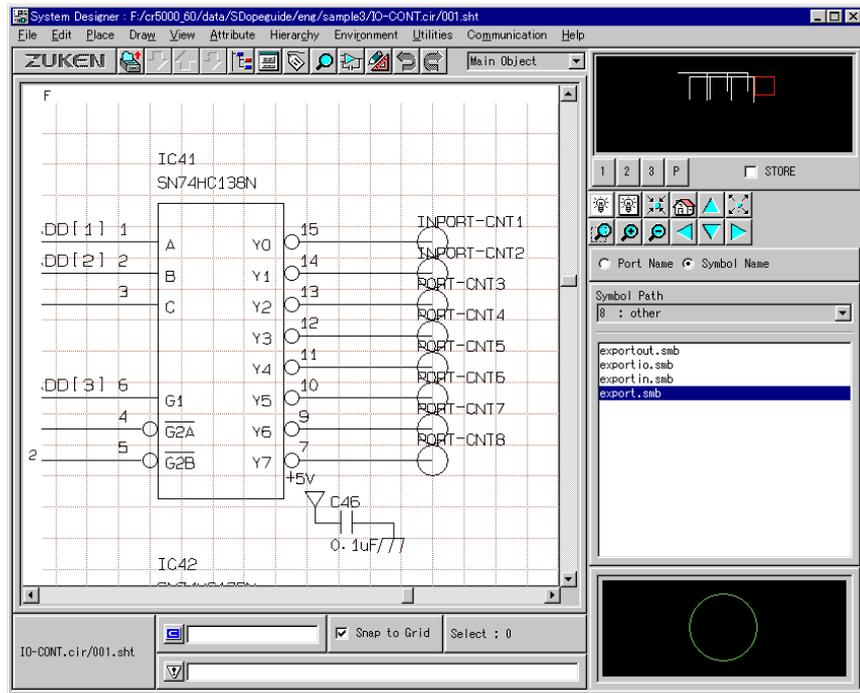
The symbols to be the hierarchical connector will be listed.



For more details on external ports, see "Block Generator Resource File" and "External port Symbols".

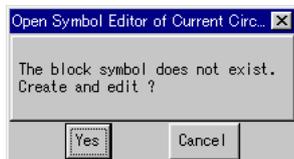
2) Input the hierarchical connector into the net end point.

If you have set the parts name of the hierarchical connector, the parts name designated here will be the pin name of the block symbol.

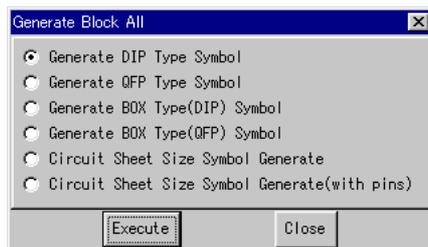


If you have the IO property set to the hierarchical connector pin, you can specify the position in which the pin for DIP Type and QFP Type occurs.

3) Specify [Hierarchy] - [Edit block symbol], or [Hierarchy] -[Generate Entry Sheet's Block] from the menu bar.



Select the type of the symbol to be created.

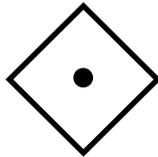


Create the block symbol in the same directory containing the subcircuit block.

**External Port Symbols*

Take note of the following points when creating external port symbols. The symbol file name is "exportxxx.smb".

Any symbol figure can be used.



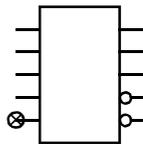
Component type: Hierarchy connector
Function type : DEFAULT LOGIC

The number of pins is 1.
The IO property can be none.

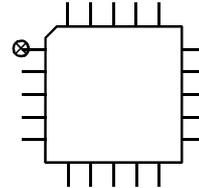
**Auto-generated Symbols*

The following six shape types of symbols can be auto-generated:

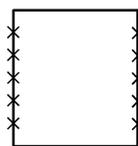
DIP symbol



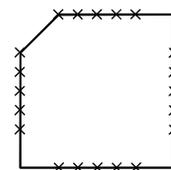
QFP symbol



Box (DIP) symbol



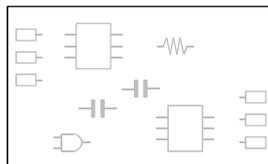
Box (QFP) symbol



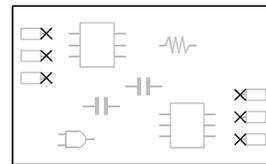
Internal circuit outline symbol

Internal circuit outline symbol (with pins)

These symbols are generated in the same size as the sheet size of the first sheet (usually 001.sht) for the internal circuit.



No pin is generated in this symbol.



Pins are generated at the same locations as hierarchy connectors.



For more detail on the parameter for the shapes of auto-generated symbols, "Block Generator Resource File" and "External port Symbols".



The parameters for the shapes of auto-generated symbols are defined in "Block Generator Resource File(geneblk.rsc)" .

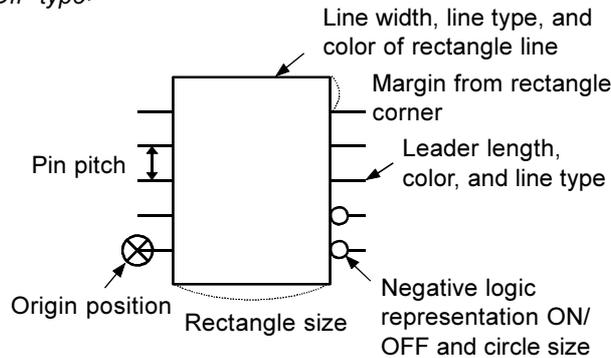
*Block Generator Resource File (geneblk.rsc)

The block generator resource file (geneblk.rsc) defines the symbol sheet names and placement methods for external port symbols to be used when the following commands are executed:

Auto-generate Outline Symbol
 Generate Template Circuit Sheet
 Block Partial Circuit
 Create HBS File

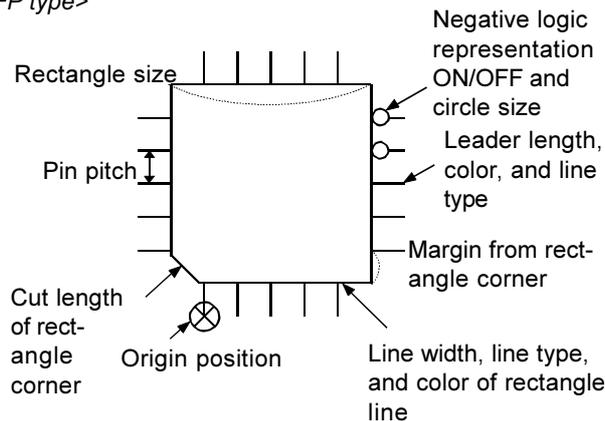
1. A set of parameters for outline symbol auto-generation can be set separately for two shape types of symbols to be generated (DIP and QFP types) as follows;

<DIP type>



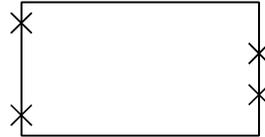
- Pin array (based on I/O property)
- For symbol and pin property viewers:
 - Font number
 - Placement position
 - Origin position
 - Angle
 - Color display ON/OFF

<QFP type>

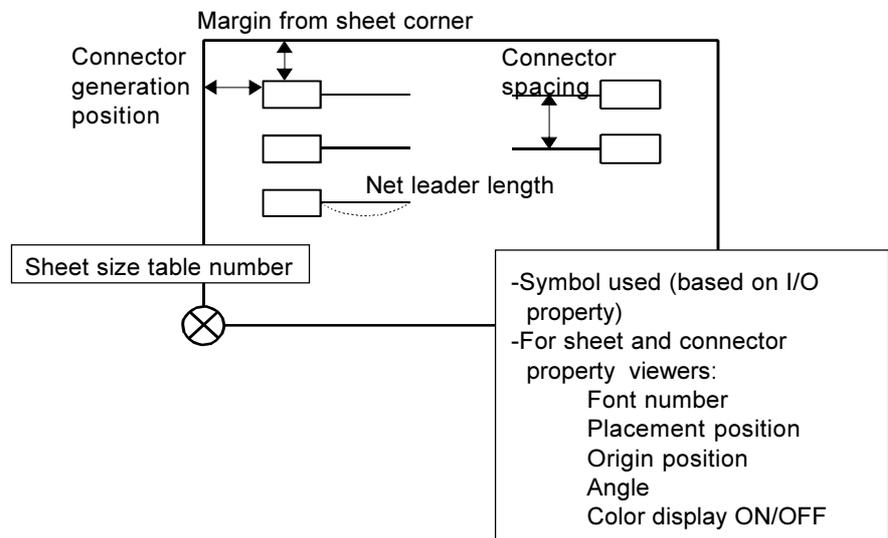


- Pin array (based on I/O property)
- For symbol and pin property viewers:
 - Font number
 - Placement position
 - Origin position
 - Angle
 - Color display ON/OFF

2. The parameters for generating partial circuit blocked symbols can specify the line type and color of the symbol outline and the external port symbol (hierarchy connector) name.



3. The parameters for generating internal circuit templates can specify the following settings:



4. The order of definitions in the HBS file can be defined.

! ATTENTION

The "I/O properties" set for external port symbol pins take effect only when a new Block symbol sheet is created. Even when you modify an already existing symbol sheet, the same I/O properties as are used for the modified symbol sheet. To recreate a symbol with new I/O properties on a schematic, delete the symbol sheet and create it again as a new one.

2. When creating a block symbol sheet with reference to the circuit already created.

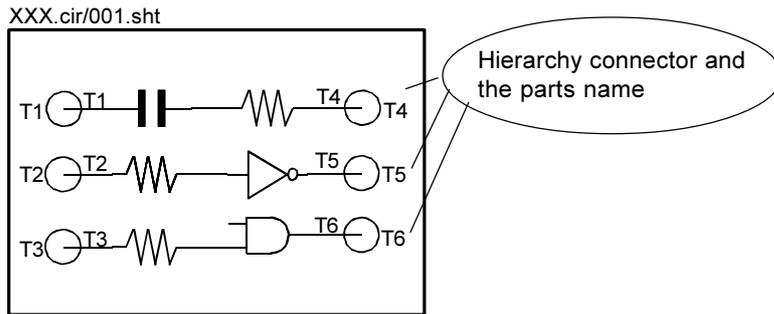
First enter the hierarchical connector in the block subcircuit, then create the block symbol.

 **EXAMPLE**

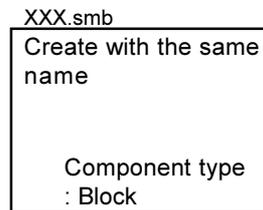
1) Enter the hierarchical connector symbol to be the pin for the block symbol into the net end point, then save the block subcircuit.

 **See Also**

See the previous section for how to enter the hierarchical connector.



2) Open the block symbol sheet (XXX.smb) with the name same as block subcircuit (XXX.cir).



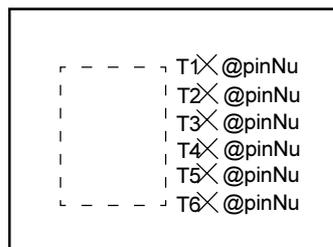
Change the sheet property and change the component type to [Block].

Block check is performed to open the file of the same name.

3) Choose [Hierarchy] - [Generate Block Symbol Pin] from the menu bar.

A pin will be created by using the hierarchical connector already entered in the block subcircuit as the pin of the symbol.

Edit the block symbol.



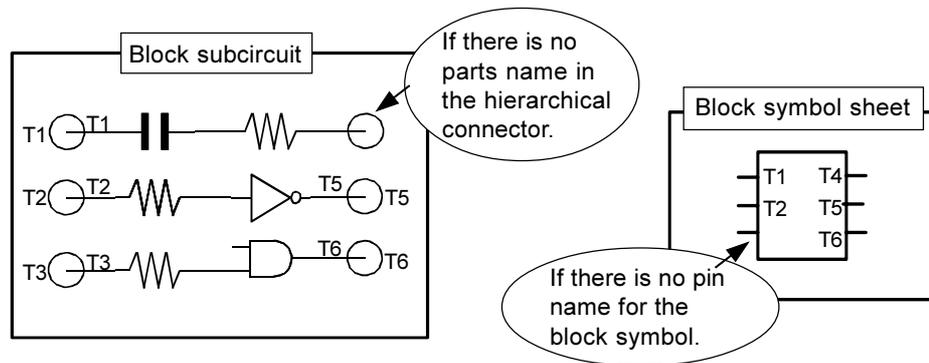
The pin is generated outside the sheet size.

*About block check

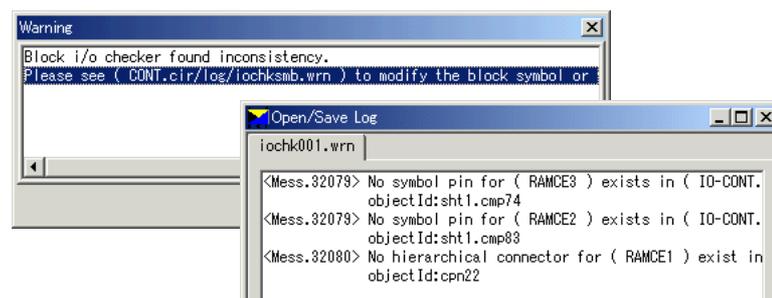
When both the circuit directory and the symbol sheet of the same name are contained in the same directory, consider them as the circuit block, and check consistency of block each time the circuit or the symbol sheet is opened or closed.

The following conditions are checked, and if something wrong exists, then a warning message appears in the dialog.

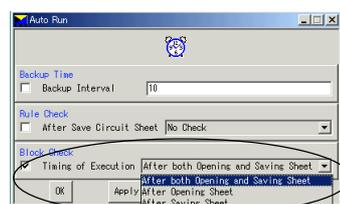
- 1.If the hierarchical connector of the subcircuit block has no name
- 2.If there is no pin name of the block symbol corresponding to the hierarchical connector of the subcircuit block.
- 3.If there is no pin name for the pin of the block symbol.
- 4.If there is no hierarchical connector of the subcircuit block corresponding to the pin of the block symbol.



You can confirm the details of the warning message by choosing [Utility] - [Open/Save Log Check] from the menu bar.



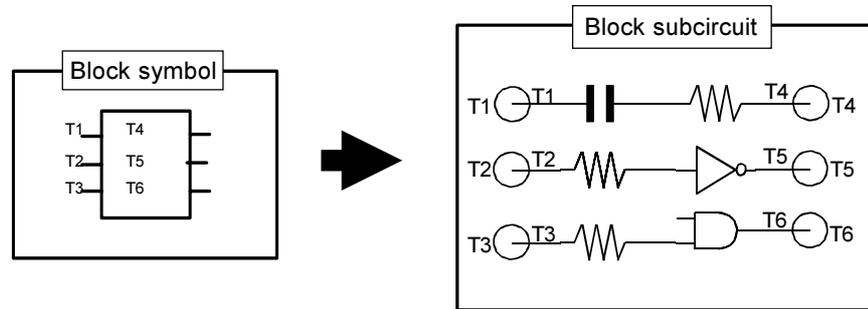
When a warning message appears, edit the subcircuit block or block symbol.



You can specify the timing of checking in the environment resource file.

● **Creating a block top-down**

How to create a block subcircuit from a block symbol.

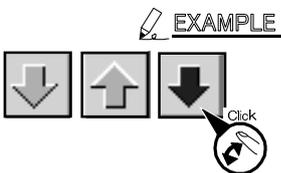


The following methods are available for creating a symbol entered in the circuit or creating an already created symbol, or a new symbol, thus creating a circuit block.

1. Create the block subcircuit of the symbol residing in the circuit.
2. Create the subcircuit from an already created symbol sheet.
3. Create the subcircuit from a symbol sheet being edited.
4. Create a symbol on the circuit and sheet, then create the subcircuit.

1. Creating the block subcircuit of a symbol residing in the circuit.

1) Select the symbol used to create the subcircuit.

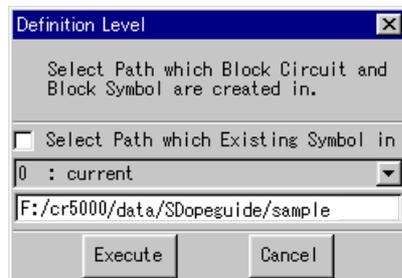


Specify [Hierarchy]-[Push Definition] from the menu bar.



The dialog indicating the switch to the Definition Level is displayed.

2) Specify the directory in which the block subcircuit and the block symbol will



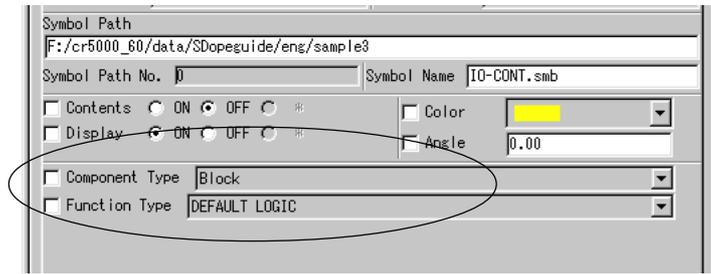
Check off if you want to create the subcircuit in the same path as the symbol.

The directory of the selected path will be displayed.



The path displayed here is the symbol defined in Data Resource File (landata.rsc).

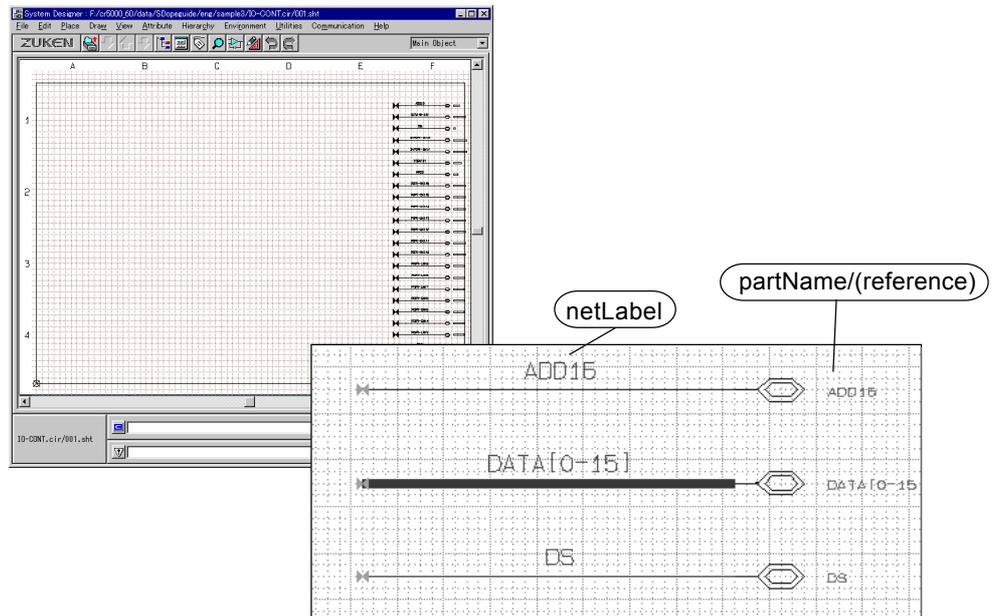
Component type of the indicated component is changed to [Block].



Up to this point, the following steps have been taken.

1. Copy the symbol sheet to the specified directory.
(If a path different from the one containing the symbol is specified)
2. Create the subcircuit directory (symbol name.cir) in the specified directory.

4) The template sheet of the created block subcircuit opens to edit the block subcircuit.



The template sheet of the block subcircuit will be created under the condition such that the hierarchical connectors in number of pins set in the symbol and the net connected to the hierarchical connectors are input. netLabel is added to the net, and partName and (Reference) are set to the hierarchical connector. In addition, you can set whether or not to reference added to the hierarchy connector is added to the block generator resource file (geneblk.rsc).

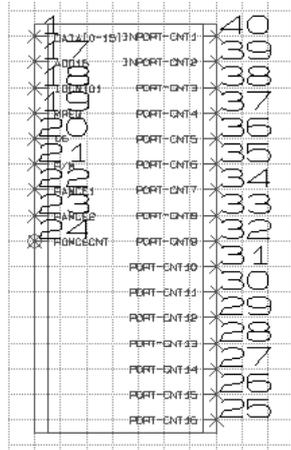


The parameters for the subcircuit template are set in the Block Generator Resource File (geneblk.rsc).

2. Creating the subcircuit from an already created symbol sheet

Create a block symbol, and create the subcircuit template based on the block symbol.

1) Set and save the pinLabel for the pin of the block symbol.



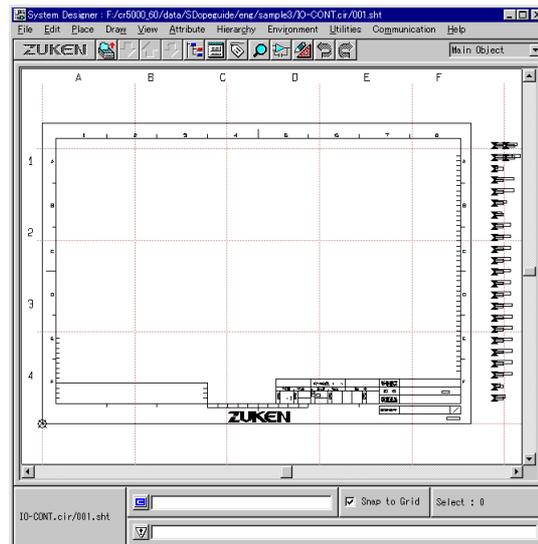
2) Open the circuit directory of the name same as the block symbol.

To open the file of the same name, block check is performed.

3) Specify [Hierarchy] - [Generate Block Hierarchical connectors] from the menu bar.

As the hierarchical connector, the pin already input to the block symbol will be generated.

Edit the subcircuit block.

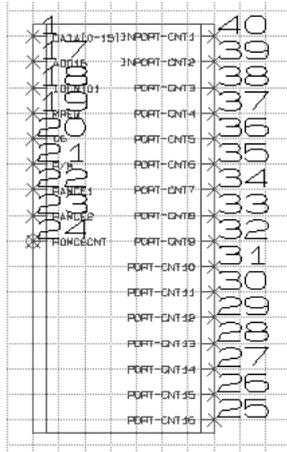


Hierarchical connector is generated outside the sheet size.

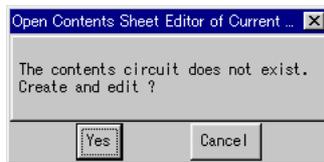
3. Creating the subcircuit from a symbol sheet being created

While creating a block symbol, create the subcircuit template based on the block symbol.

1) Set the pinLabel to the pin of the block symbol.

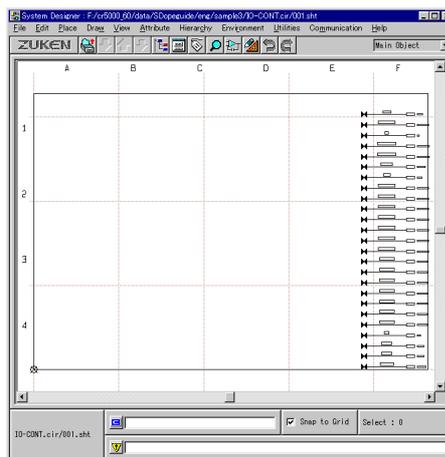


2) Specify [Hierarchy] -[Edit Contents Circuit] from the menu bar.



At the hierarchical connector, the pin already input to the block symbol will be generated.

Edit the subcircuit block.



4. Creating a block symbol and a block subcircuit within the schematic sheet

When editing the schematic sheet, create a block symbol sheet from the dialog used for symbol creation. At this time, no symbol editor will be used.

1) Select [Hierarchy] - [Generate Sheet Symbol] from the menu.

The generate sheet symbol dialog appears.

It specifies the path for storing the block. (A symbol path is displayed as a choice).

Specify the block name (Symbol name is created with same name, too.)

If Repeat is ON (), you can be inputted continuously by the same establishment.

Specify the comment

Specify the number of each pin

Delete the condition defined

Close this dialog

Input the symbol shape with the defined condition

Open the dialog for define the attribute such as a pin label

ID	Pin Label	IO	Bit width
-	A	INPUT	1
-	B	INPUT	1
-	C	INPUT	1
-		INPUT	1
-		OUTPUT	1
-		OUTPUT	1
-		OUTPUT	1

Move the cell of the focus pin to top and button

Add the pin of the attribute which is the same as focus pin cell. It is increased on the pin label when the end of the pin label is a number.

Delete the cell of the focus pin

The attribute of this cell is changed by double-click.

When the symbols are created, Pin IDs are assigned to the pin setting column in descending order. Inserting is not available.

2) Set the attribute of the pin.

Path: 0 : current

Block name: tpdwn Repeat

Comment: top

Input pins: 4

Output pins: 4

Bidirect pins: 0

Buttons: Place, Close

Click the [Place] button.

! ATTENTION

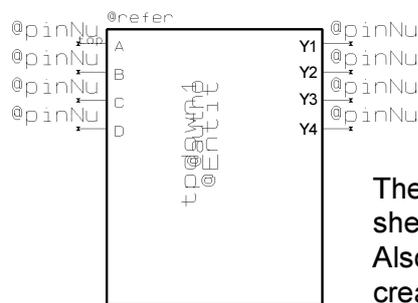
In case that pin name is not entered, symbol shape can not be created.



3)Specify the symbol shape

The cross cursor to input the symbol shape when a cursor is taken onto the canvas is indicated.

Insert a rectangle which become the symbol shape.



The symbol is created on the circuit sheet.

Also, the symbol sheet (XXX.smb) is created.

The following work is executed by operations step 1 to 3.

A symbol having the following attributes is created under the specified path.
the symbol attribute

Component Type	:	Block
partName	:	Block File Name
Comment	:	Component Comment

4) The internal circuit directory is not created yet.

Select the symbol, and then choose [Hierarchy] - [Push Definition] on the menu bar to edit the block subcircuit.

The following work is executed by the operation .

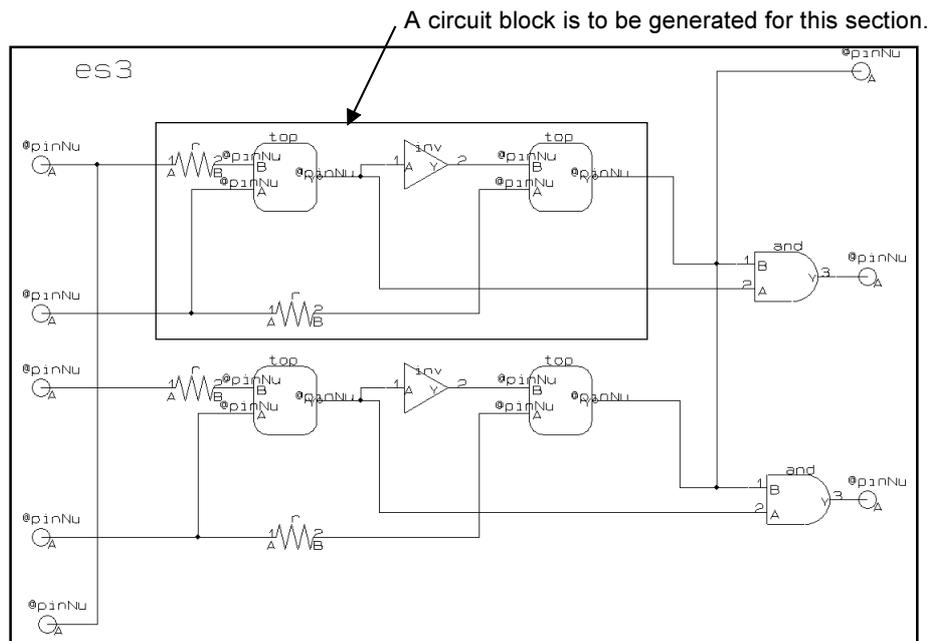
1.The block subcircuit directory, represented by "symbol name.cir," is created in the specified directory.

● Sharing Circuits

It is common in circuit design to standardize a part of the circuit for performing a specific function and to share this sub-circuit both within the overall circuit and between designers. In this way, rather than breaking the entire circuit into blocks, sections of the circuit can be set as circuit blocks and these blocks shared. In this case, the circuit section being defined as a circuit block is automatically created as a new schematic directory. The outline symbol sheet and block file are also generated automatically.

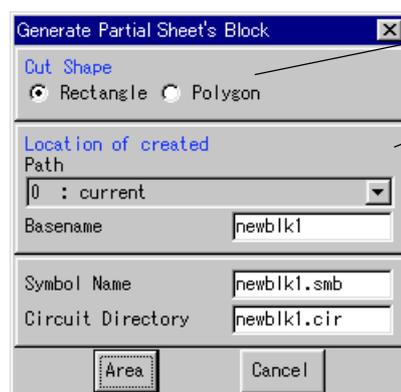
 **EXAMPLE**

1) Open the schematic to use for generating a circuit block .



2) Select [Hierarchy] - [Generate Partial Block] from the menu.

The Block Partial Circuit dialog appears.



Specify the cut figure.

Choose one, where you store the block, from the list of symbol paths.

Specify the names of the files to be created.

Use sub1 as the base name. This changes the file names to sub1.

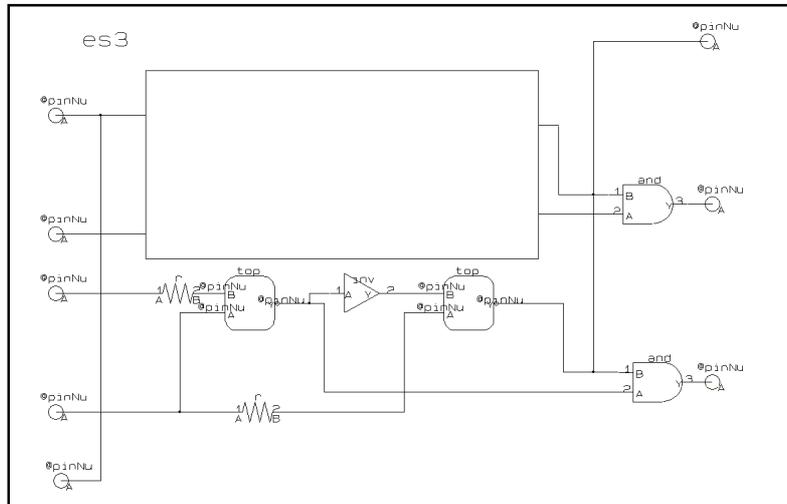
Click [Area].

The shape selected in the sheet editor specifies the section of circuit to be generated as a block.

 **NOTE**

Symbol paths defined in the data resource file "landata.rsc" are listed for your choice.

3)The specified section on the schematic sheet changes to a circuit block.



At this time, the internal circuit directory (sub1.cir) and outline symbol sheet (sub1.smb) are created in the same directory level.

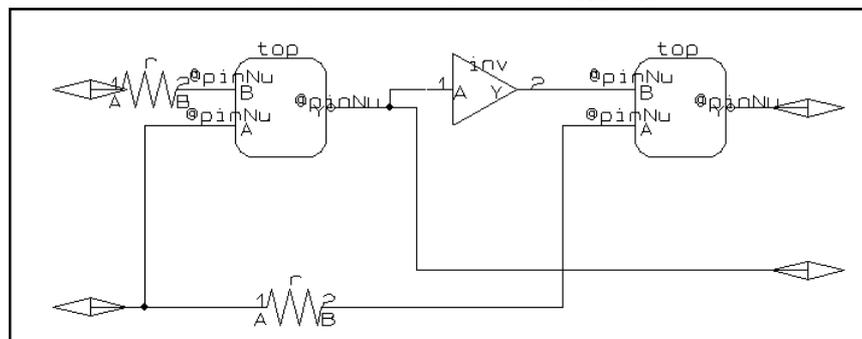
Block symbol sub1.smb



Schematic directory

The external port symbols are input.

sub1.cir



ATTENTION

The external port symbols to be input are set in the resource file (geneblk.rsc).

3. Editing the Circuit Block

● Input Circuit Block

Input an already created circuit block into the schematic sheet.
The component entered as a circuit block holds the instance information at lower hierarchical level.

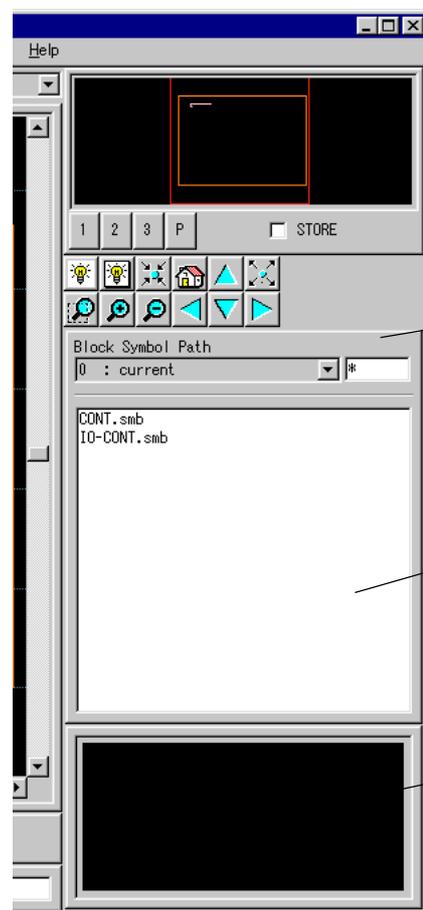
It is possible to input the same circuit block on the same sheet.

You can move to the Definition Level and the Instance Level from the schematic sheet.

To output a net list, lower hierarchical levels will be expanded.

The entered block symbol will be set to "Component type: Block".

- 1) Open the schematic sheet which you will input the circuit block.
Select [Place] - [Circuit Block] from the menu.



Specify the circuit block path(symbol search path).

File name list box
If a circuit directory and a symbol sheet of the same name reside under the circuit block path directory (symbol path), both the block symbol and the directory will be displayed.

Displays the shape of the Block symbol .

- 2) The same operation as that of symbol figure input will be used for arrangement on the schematic sheet.

 **NOTE** Operation for move and erase is the same as that for other objects.



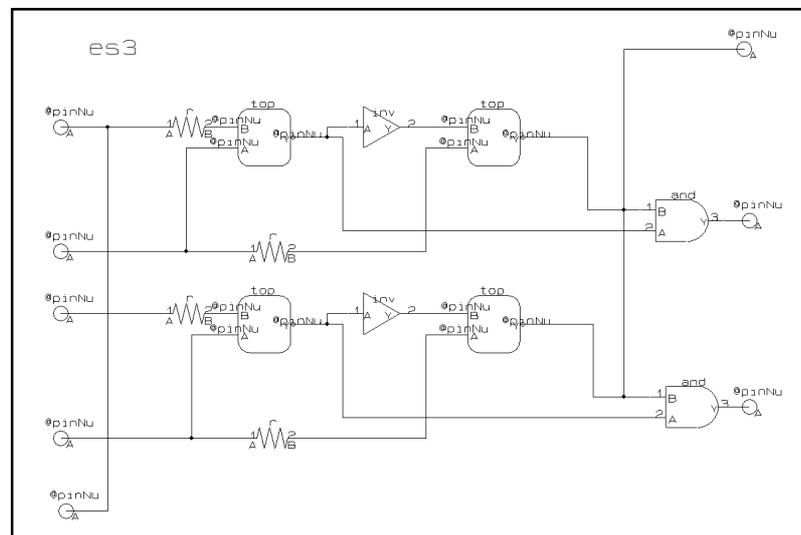
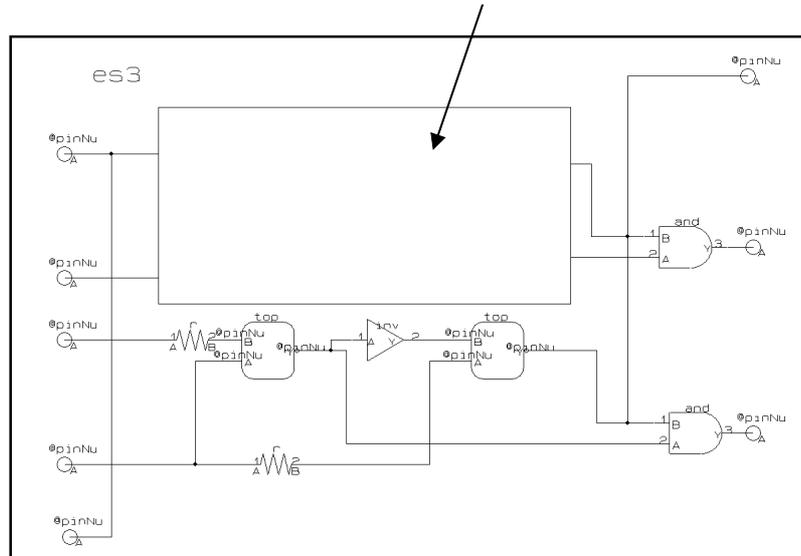
● Expand the Circuit Block

Expand the circuit block entered in the schematic sheet.
 (Use care that once the circuit block is expanded, it cannot be restored.)
 The block subcircuit expanded will be treated as individual components.



1) Select the circuit block to expand.

Select [Hierarchy] - [Break Circuit Block] from the menu.



ATTENTION

Connections are made when the connection pins for the expanded circuit and unconnected net terminals are at the same point. The instance information is also expanded directly on the sheet.

Expansion does not occur in the following cases:

- The sheet size of the internal circuit is larger than the symbol sheet size of the circuit block.
- When the internal circuit has more than one sheet.

● Editing the Circuit Block

This section refers to the following three methods for proceeding with circuit design using the circuit blocks.

1. Edit the circuit block created in Generate Sheet Symbol.
2. Edit the circuit block at the Instance Level.
3. Edit the circuit block at the Definition Level.

1. Edit a circuit block created by generate sheet symbol.

Edit a symbol created by generate sheet symbol on the circuit sheet. The symbol sheet is edited simultaneously.

- 1) Select the symbol generated by Generate Sheet Symbol. Select [Hierarchy] - [Edit Sheet Symbol] from the menu.

The addition : deletion of the pin count, pin property(Pin name:IO :Bit width) can be changed.

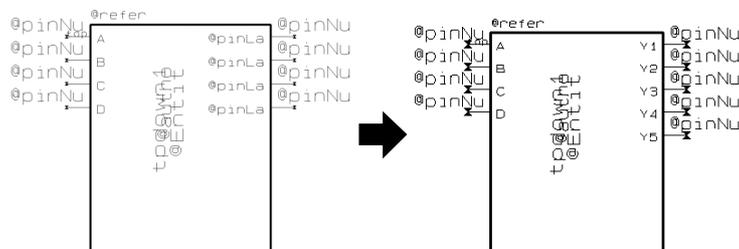
The screenshot shows the 'Edit Sheet Symbol' dialog box with the following callouts:

- Specify the comment**: Points to the 'Comment' field.
- Move the cell of the focus pin to top and bottom**: Points to the 'Up' and 'Down' buttons.
- Add the pin of the attribute which is the same as focus pin cell. It is increased on the pin label when the end of the pin label is a number.**: Points to the 'Append' button.
- Delete the cell of the focus pin**: Points to the 'Delete' button.
- Reset the condition before editing**: Points to the 'Reset' button.
- The attribute of this cell is changed by double-click.**: Points to a cell in the 'Set Pins' table.

ID	Pin Label	IO	Bit width
1	A	INPUT	1
2	B	INPUT	1
3	C	INPUT	1
4	D	INPUT	1
5	Y1	OUTPUT	1
6	Y2	OUTPUT	1
7	Y3	OUTPUT	1
8	Y4	OUTPUT	1

Click the [OK] button or the [Apply] button.

2) The symbol sheet is changed.



The symbol will be changed but no change will be reflected on the block subcircuit.

It is necessary to edit the block subcircuit because there is inconsistency with the block.

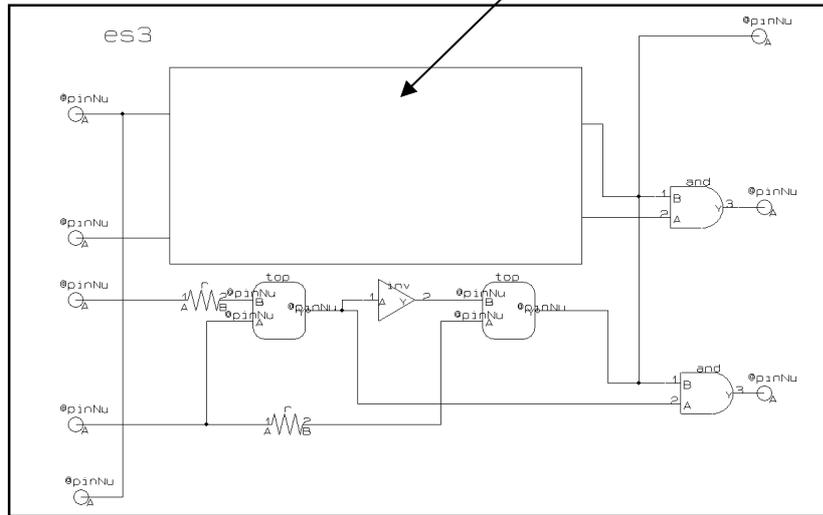
2. Edit a circuit block in the instance hierarchy.



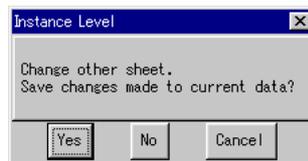
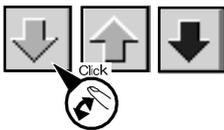
Editing a circuit block in the instance hierarchy only edits instance information and changes the properties only.



1) Select the circuit block on the schematic sheet for which you wish to edit instance information.



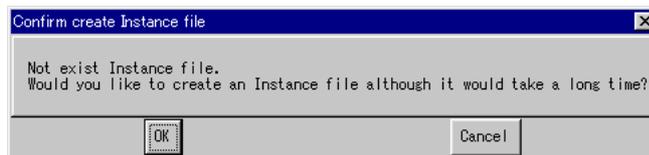
2) Select [Hierarchy] - [Push Instance] from the menu.



Click [Yes].



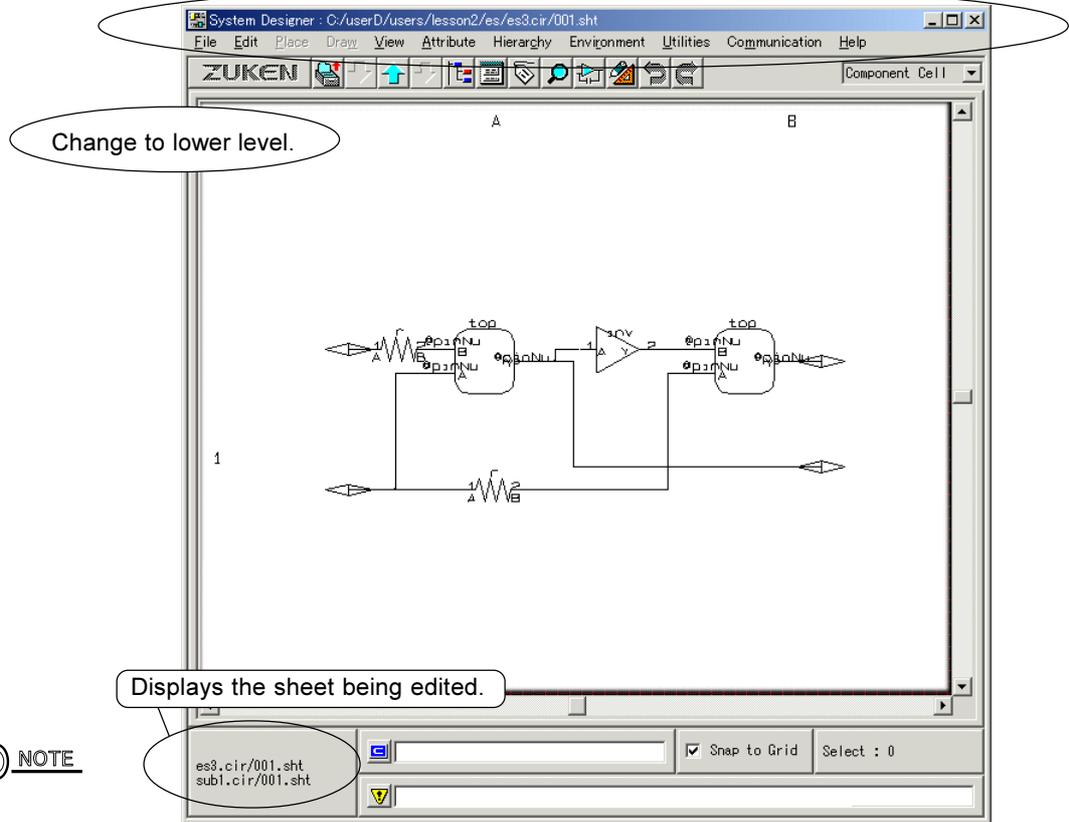
When the instance information file (instance) underneath the schematic directory does not exist, the following message is output.



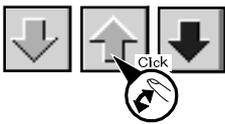
Clicking <<OK>> lets you create the instanc file and move to the Instance Level. Clicking <<Cancel>> also cancels the move to the Instance Level.

3) You can now edit the internal circuit sheet.

Unavailable commands appear grayed.



NOTE



4) When you have finished editing, select [Hierarchy] - [Pop Block] from the menu.

ATTENTION In this case, you do not need to save your work.

NOTE You can display the property value within the instance hierarchy from the display contents.

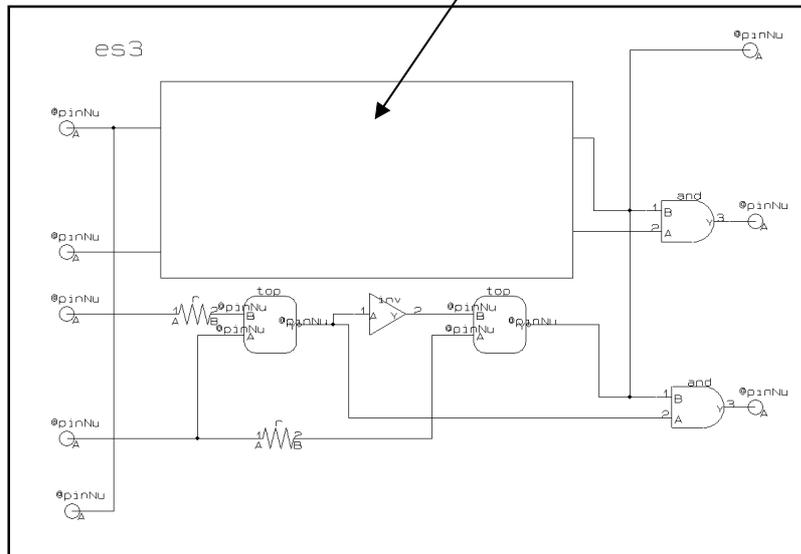
3. Editing the Circuit Block

3. Edit a circuit block in the definition hierarchy.

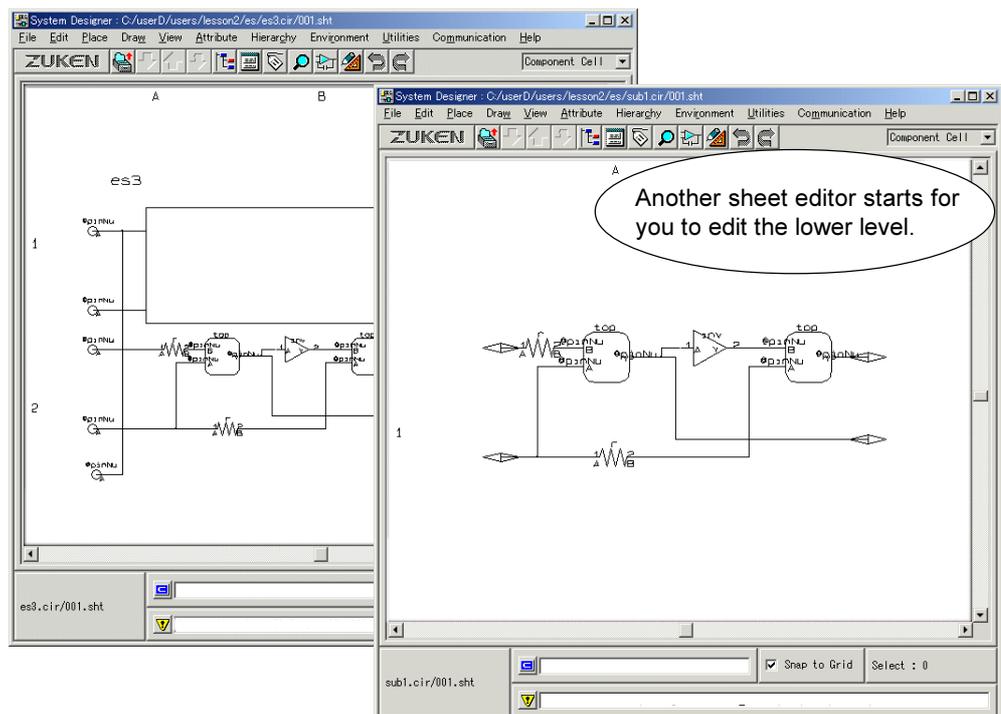
Editing a circuit block in the definition hierarchy edits the lower level schematic directly. Therefore, another sheet editor starts.



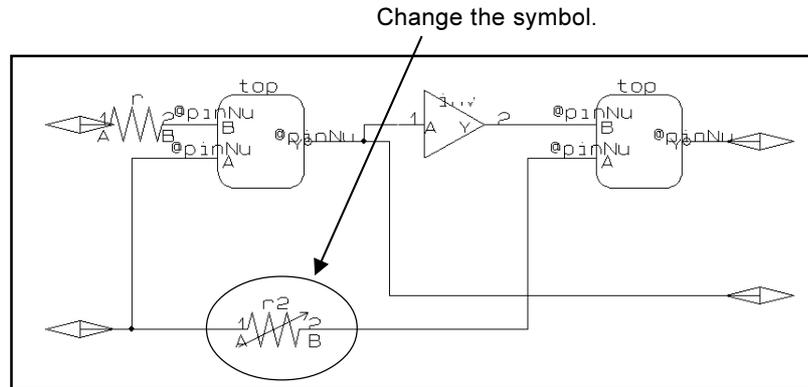
1) Select the circuit block on the schematic sheet for which to edit the internal circuit.



2) Select [Hierarchy] - [Push Definition] from the menu.



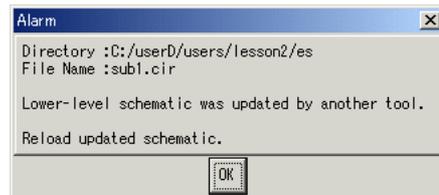
3) Edit the circuit.



ATTENTION

When changing circuits in the definition hierarchy, note that changing the sheet size and position of net terminals in particular, results in the system being unable to perform internal display of the circuit block or to expand the circuit block.

4) Save the edited file.



Changing any circuit in the definition hierarchy opens the dialog on the left.

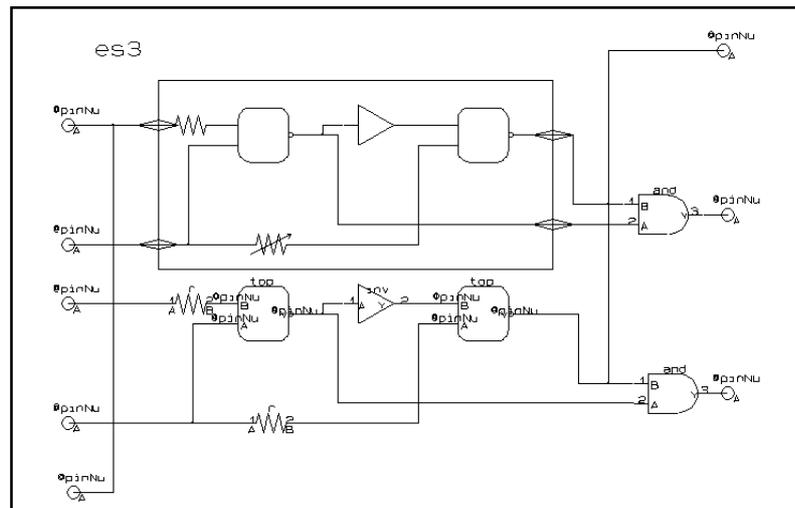
ATTENTION

You cannot move to a higher level in the definition hierarchy.

5) The edited circuit block is updated in the higher level.

To check, display the internal circuit of the circuit block.

Select [Hierarchy] - [Display Contents] - [ON] from the menu.



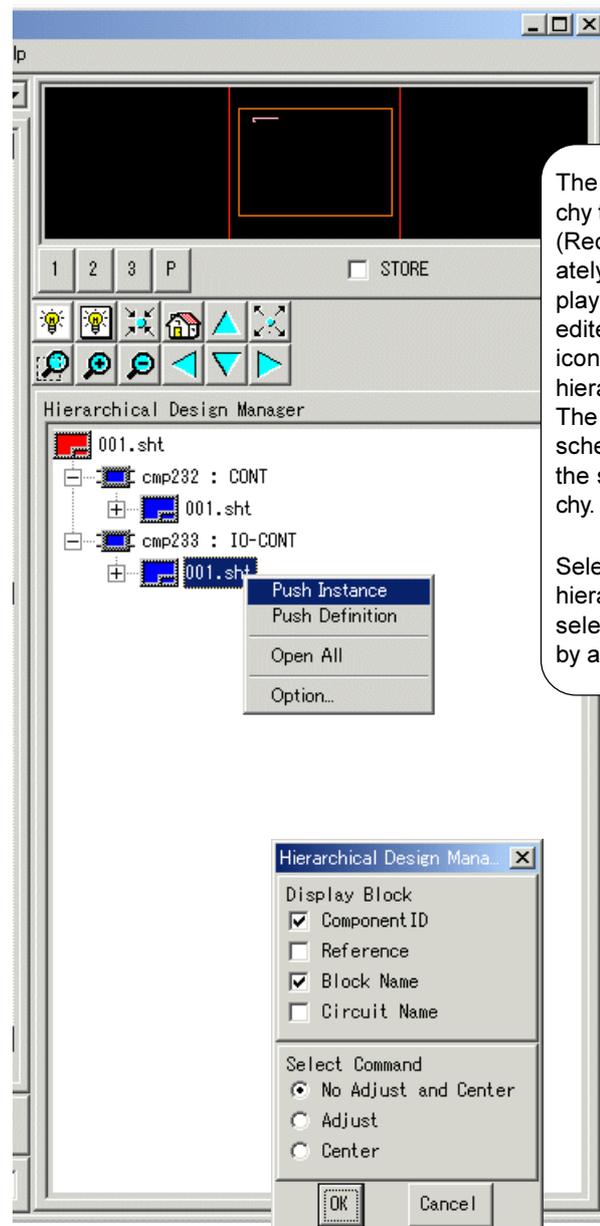
**Hierarchical Design Manager*

The structure of the hierarchical circuit design can be displayed as a hierarchy tree by the Hierarchical Design Manager. You can use this to view the circuit being edited, the overall hierarchy, and the position of the circuit in the hierarchy.

Also, by selecting a circuit block from the hierarchy tree, you can change the circuit being edited to any schematic sheet from any level in the hierarchy.

The Hierarchical Design Manager appears as a panel menu.

Select [Hierarchy] - [Hierarchical Design Manager] from the menu.



The hierarchy is displayed as a hierarchy tree.
 (Red icon: Only the hierarchy immediately below the highest level is displayed when the circuit currently being edited is started. Double click on each icon to display the lower levels of the hierarchy.)
 The reference, block file name, and schematic directory are displayed for the selected circuit block in the hierarchy.
 Select whether to display in the hierarchy tree. If two or more items are selected, the names appear delimited by a colon ":".

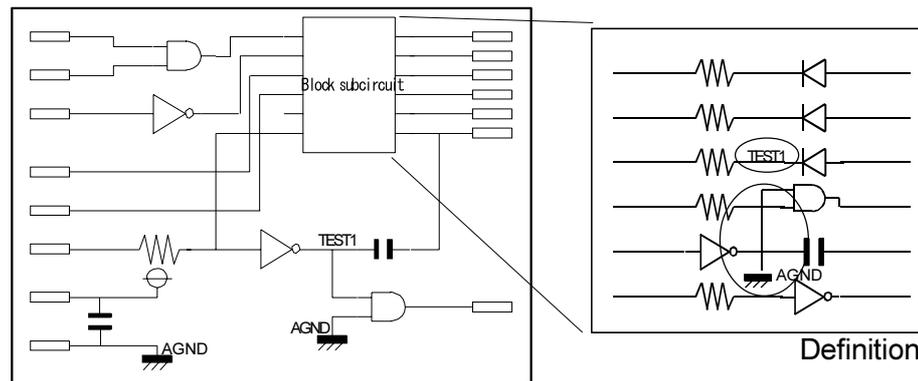
You can move from the assist menu to the Definition Level or the Instance Level by specifying the sheet file.

From the assist menu, you can specify the method for block display in the option dialog and the display method used when the block symbol is selected

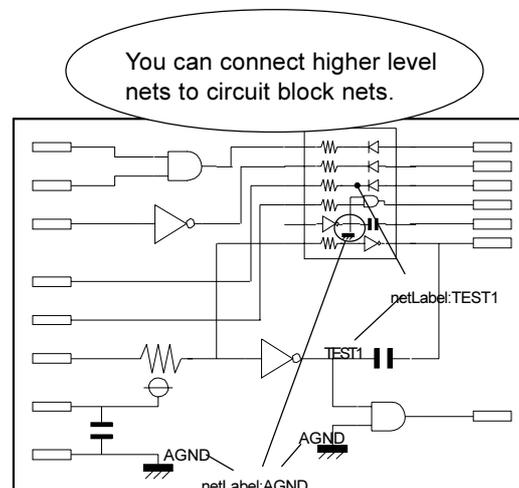
● Nets that Connect between Levels

In hierarchical design, you can connect nets between levels.

In a hierarchical design, net names in circuit blocks are instance information and the net names are automatically added by the system (they cannot be edited). Therefore, if both the higher level and the Definition Level are set to the same net name, they will be output as different nets for net output. (It is because the net is output at the Instance Level.) However, by setting the global flag [ON], the net name can be saved unchanged and be treated as the same net in the net list.



- Set the Global flag [ON] for the circuit block's internal net name "TEST1".
- Set the Global flag for Power/Ground [ON] for the circuit block's internal symbol.



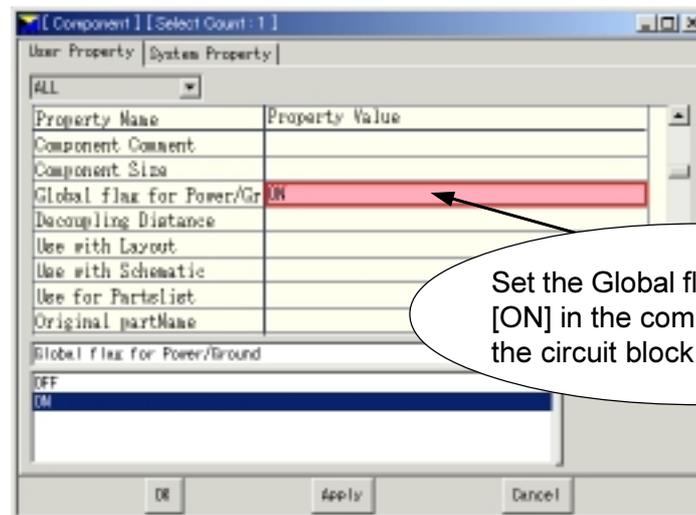
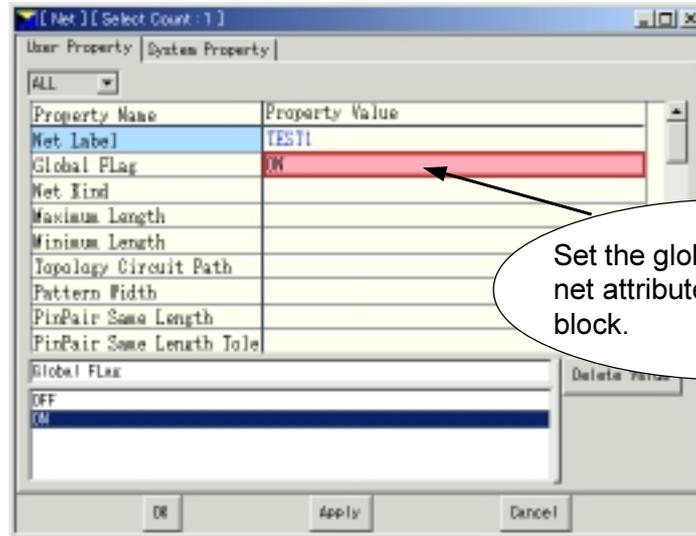
The global net flag includes the net property "Global Flag" for general nets and the component property "Global flag for Power/Ground" used for power/ground nets.

Because Power/Ground Net uses "partName" of the Power/Ground Component as the net name, setting will be made as the component property instead of the net property.

You can also set the "Global flag for Power/Ground" to the sheet connector.

3. Editing the Circuit Block

 **EXAMPLE** When creating the internal circuit for a circuit block or editing in the definition hierarchy, give nets the same name as the nets you wish to connect to in the upper level circuit.



*Block Generator

Block Generator allows you to:

- Edit circuit block files (xx.blk)
- Create outline symbols
- Create internal circuit templates
- Create HBS files

Choose [circuit directory / symbol sheet] with Design File Manager, and then choose [Tool] - [Action] - [Block Generator] on the menu bar.

The screenshot shows the 'Block Generator' dialog box with the following callouts:

- Allows you to specify a symbol shape of a block symbol to be generated automatically.** (points to the 'Symbol Name' field)
- Toggles the internal circuit/symbol sheet display between ON and OFF.** (points to the 'View Figure' checkbox)
- Sets an appropriate open mode automatically. The commands available vary depending on the current open mode.** (points to the 'Open Mode' dropdown)
- Displays the block Symbol sheet .** (points to the 'Symbol Name' field)
- Displays the internal circuit directory name.** (points to the 'Circuit Directory' field)
- Changes the sheet to be displayed.** (points to the 'Sheet Name' field)
- Displays the symbol shape specified by the symbol name.** (points to the 'Symbol Figure' preview area)
- Displays xxx.sht in the internal circuit directory.** (points to the 'Sheet Name' field)
- Lists the connections between outline the symbol sheet pins and the internal circuit.** (points to the 'Pin Assignment' table)
- Defines or deletes pin assignments.** (points to the 'Pin No.' and 'Net Name' fields)
- Displays the number of pin assignments defined.** (points to the 'No. of Pin Assignments' field)
- You can change the internal circuit and symbol figure display.** (points to the 'Redraw', 'Display All', 'Zoom In', and 'Zoom Out' buttons)
- Position the cursor in the display area and click the right mouse button.** (points to the 'Symbol Figure' preview area)

See Also

For details, access online Help.

NOTE

If a symbol file exists when symbol auto-generation is executed, the existing file is renamed as a backup file. That is, the symbol file existing immediately before auto-generation is saved and thus can be restored.

Existing file "btup2.smb" Renamed to "#btup2.smb"

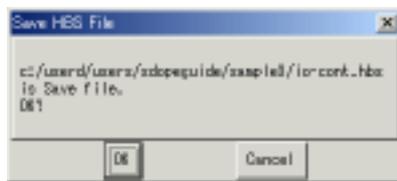
*HBS File

The HBS file is a file in the CSV (comma separated value) format, which is not used for exchanging data directly with System Designer. The HBS file is used for extracting a block property file from VHDL or VerilogHDL to generate symbols and blocks.

 **EXAMPLE**

Output an existing circuit block to an HBS file.
From the menu bar of Block Generator, select File Save HBS File .

The confirmation dialog is displayed.



The HBS file is created with a file name of "block-filename.hbs".

```
"sheet"  
"pin:1" ,"BIDIRECT","NET1"  
"pin:2" ,"BIDIRECT","NET2"  
"pin:3" ,"BIDIRECT","NET3"
```

"Pin ID", "I/O property", "Terminal name (net name)"

Generate a symbol from an existing HBS file.
From the menu bar of Block Generator, select File Save HBS File .



Select xxxx.hbs.

Appendix

● Circuit blocks created by using Rev.5.0 or earlier

Circuit blocks created by using Rev.5.0 or earlier differ in structure from those circuit blocks created by using Rev6.0.

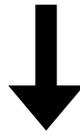
Rev5.0 or earlier

Consisting of the following three parts:

Block file	xx.blk
Block subcircuit directory	xx.cir
Block symbol sheet	xx.smb

Other circuit block-related information

The following properties in the block symbols are used.
Subcircuit path number
Block file name
The following properties are used for pins of the hierarchical connector.
External pin index



Rev6.0 or later

The block file is eliminated.

Consisting of the following two parts:

Block subcircuit directory	xx.cir
Block symbol sheet	xx.smb

Other circuit block-related information

Properties within the block symbol are not used.
Properties of the pins in the hierarchical connector are not used.

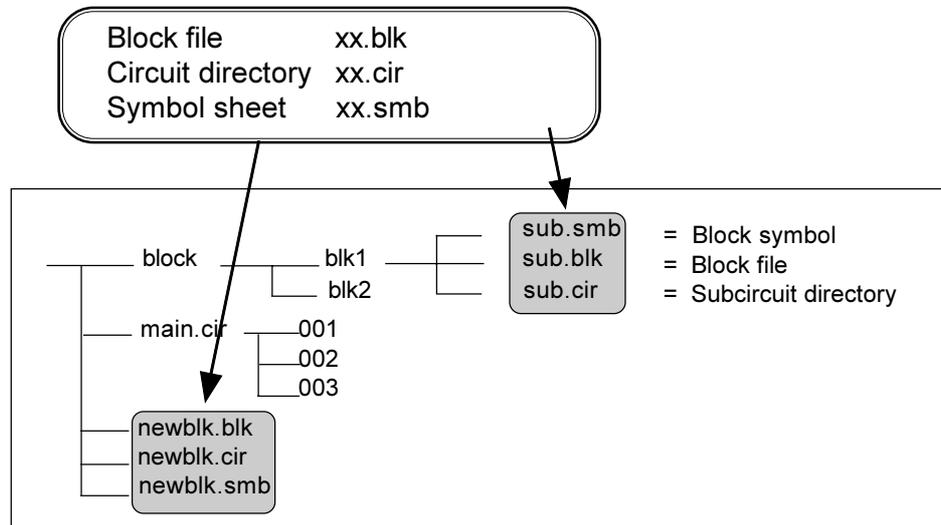
● Circuit blocks created by using Rev5.0 or earlier may be used with the usual procedures, but it is recommended that the existing blocks be replaced with those in a new structure in order to meet the need for functional improvements in the future.

● For circuit blocks convertible to the structure used in those releases after Rev6.0, the block file will be deleted when the schematic sheet or the symbol sheet is saved. In addition, the warning message will be output for those inconvertible circuit blocks.

● Processing circuit block data conversion

Two examples shown below refer to the conversion of circuit blocks created by using Rev5.0 or earlier.

1. When the following three entries are in the same directory and of the same name.



Consistency check will be performed when opening the block symbol (xxx.smb) or the subcircuit sheet (xxx.cir/001.sht).

(1) When no error was found in consistency check:

Delete the block file (xxx.blk).

Delete only when no error was found in consistency check performed when the subcircuit sheet or the block symbol is saved.

*The block file name set in the block symbol and the subcircuit path number will remain unchanged. Previous settings which still remain will cause no harm to the operation.

(2) When an error was found in consistency check:

No block file will be deleted.

Take the following steps to recover depending on error contents.

● When using the part name of the hierarchical connector:

Open the block symbol and proceed with [Generate Block Symbol Pins].

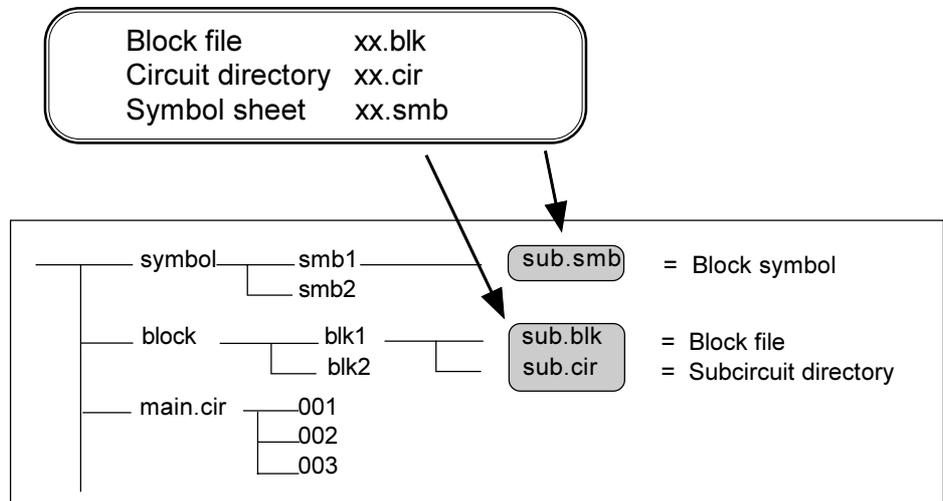
● When using the pin name of the block symbol:

Open the subcircuit sheet and proceed with [Generate Block Hierarchical Connectors].

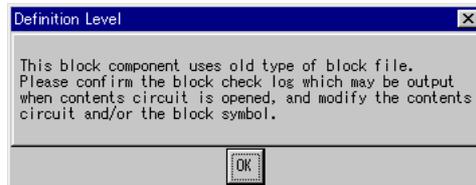
● When using the pin name of the block symbol and the net name to be connected to the hierarchical connector:

Open the subcircuit sheet and set the part name to the hierarchical connector by specifying [Place]-[Net/Bus Label].

2.If a block file and a subcircuit directory are in the same directory and the block symbol is in a different directory:



The following message appears in a move to the Definition Level of the circuitblock.



Move block symbols or the subcircuit directory and save them in the same directory under the same name.
 If the directory containing the block file is not registered in the symbol path, add it to the data resource file/symbol search path.

