



EDIF200 Schematic Converter Module Reader

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Chapter 1 What is EDIF reader ?

This software generates the circuit data of CR-5000 System Designer from EDIF(Electronic Design Interchange Format) Version 200. Please confirm the adjusted vendor and version of this software, because the contents of the EDIF file differ largely by the vendor, version on EDIF output side. The circuit data that has been generated is not always able to make net extraction and part table etc. So it needs to be edited by Schematic editor and LCDB editor after transformation.

1.1 Checked version and adjusted vendor

There are 2 type format in EDIF("Schematic view" and "Connectivity view"). This software transforms only "Schematic view". "Connectivity view" is generally called EDIF netlist. and this dosen't include figure data.

EDIF reader checks version and output program name in EDIF file and automatically recognizes which vendor the file belongs to, then performs transformation.

The following is vendor name and version of adjusted EDIF in this program.

vendor	version
VIEWLOGIC(Power view)	5.0 7.5.p
MENTOR	8.5 8.6

The above version is described in EDIF and it is sometimes different from vender's system version.

There is a possibility that some formats cannot be transformed.

Chapter 2 Functions

EDIF reader has following functions.

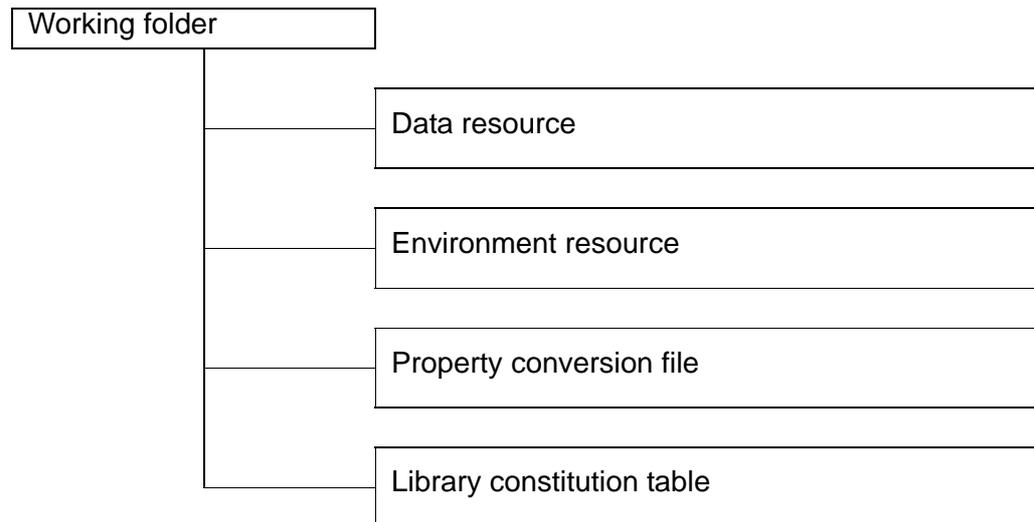
- (1) Pre-check for import
- (2) Generation of LCDB template
- (3) Generation of Symbol/Circuit sheet

Working folder^a is the folder where EDIF file exists folder.

^a.It means "Directory" in UNIX

2.1 Pre-check for import

Whole EDIF file is loaded and properties and cell constitution are checked. And also, the following files needed for transformation are generated in Working folder.



(1) Data resource

If Data resource exists in Working folder, it is not generated. If not, system Data resource is copied to Working folder.

(2) Environment resource

If Environment resource exists in Working folder, it is not generated. If not, system Data resource is copied to Working folder.

(3) Property conversion file

If Property conversion file exists in Working folder, it is not generated. If not, the template is generated.

If you make in advance a property conversion table in "\$ZCSROOT/etc/procnvTemplate.htb", when you start the [Pre-check for Import], the table will automatically be copied to the working folder.

(4) Library constitution table

library name, cell constitution and property names in EDIF file are output. This file is always regenerated by performing "Pre-check for import".

2.2 Generation of LCDB template

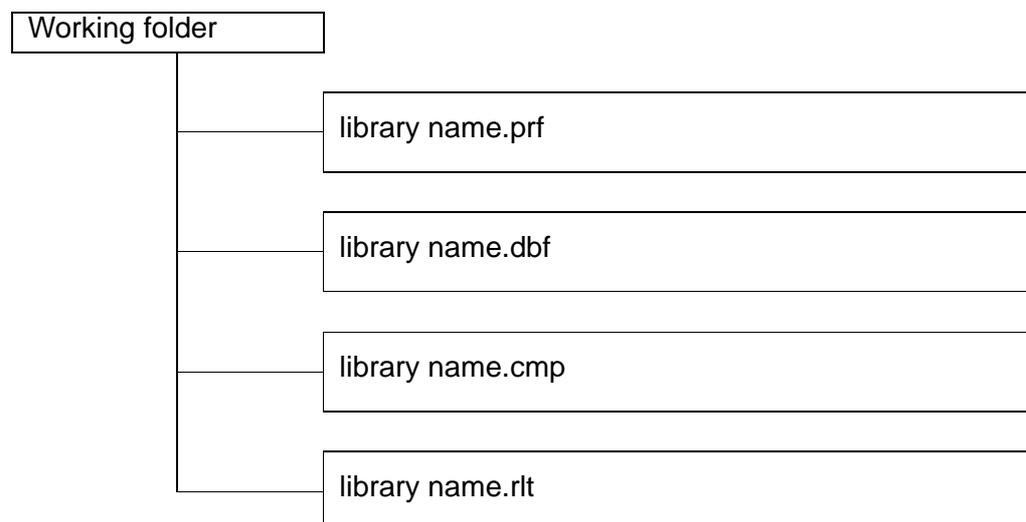
LCDB template is generated by outputting parts pin assignment information from interface description in EDIF.

The reason we use "Template" is that the EDIF where no pin assignment information is input needs hand modification.

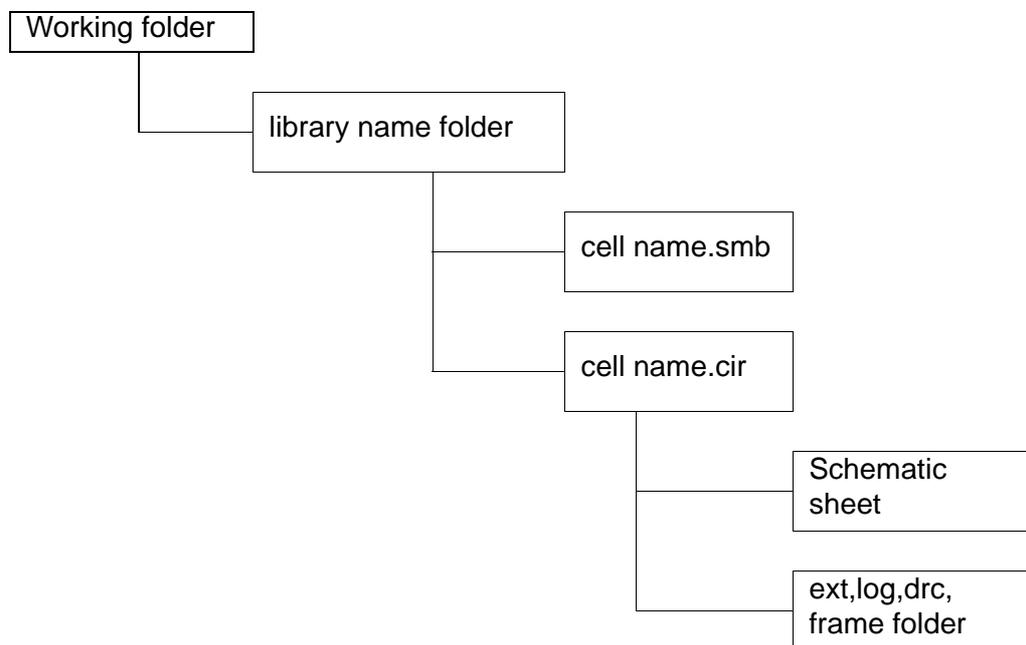
LCDB template is created as library name in working folder.

The hand modification is necessary after transformation, If there are no pin assign information in EDIF, the modification is necessary after transformation, So, it called template.

LCDB template generate in working folder.



2.3 Generat Symbol/Circuit sheet



2.3.1 Scale

Basically, conversion is performed using the scale defined in the "edif" input file. The scale specified here is determined by multiplying the scale by another scale defined in the "edif" input file.

Actual scale is determined as follows:

$$\text{Actual scale} = \text{Scale (multiplier)} / \text{Scale (divisor)}$$

When you'd like to transform a circuit on an inch grid or transform by applying a scale to the entire circuit, please use this scale value for adjustment.

For example, if you set

$$\begin{aligned} \text{Scale (multiplier)} &= 16 \\ \text{Scale (divisor)} &= 25.4 \end{aligned}$$

25.4 millimeters (1 inch) are transformed to 16 millimeters (dimension used in System Designer).

The following is described in the menu for transformation to understand easily.

Unit inside an EDIF file[] [mm] <---- scale(divisor) Unit inside System Designer[] [mm] <---- scale(multiplier)
--

Chapter 3 Operation

This chapter explains the way to operate menu and to change each setting file.

3.1 Before starting data conversion

Please confirm the following item before transformation work.

(1) hard disk space

Since this program regards the folder where EDIF exists as Working folder and creates data in that place, Please confirm the hard disk space. Though it depends on the contents of EDIF, the hard disk needs same or more space as EDIF file size to be transformed.

(2) Memory

In case of UNIX, there is a possibility that large data cannot be transformed, because memory size one process can used is limited. (In case of HP, default limit is 64M byte)

In this case, please change system setting.

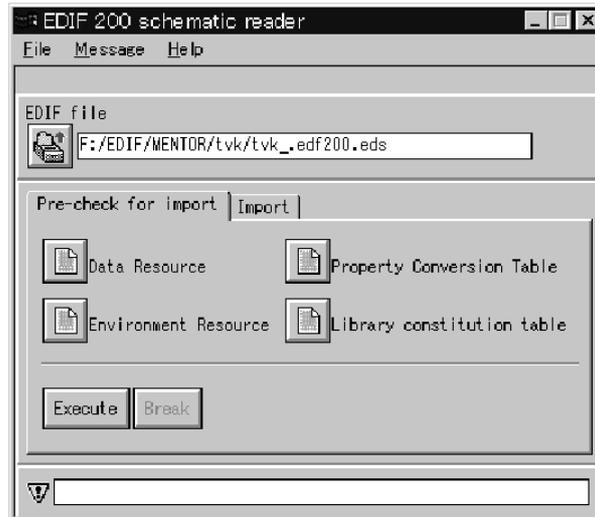
About 1/3 memory of EDIF file size is necessary large data transformation.

(3) License

EDIF reader is option software(ZX0311)

3.2 Start of program

On System designer's file manager, Select a target EDIF file in Working folder and start "EDIF 200 schematic reader" from menu Action. EDIF 200 schematic reader is displayed only at the time of file type is .edf or .eds.



If the extension of the EDIF file is not ".eds" or ".edf", you can launch the program from the [Import] menu in the File Manager by specifying the file name.

3.3 Pre-check for Import

Select Menu tab "Pre-check for Import

Execute button

By clicking "Execute" button, EDIF file is read and pre-check is performed and 4 files necessary to transformation are prepared.

In case that there is an error file when the "Pre-check for import" completes,"an error file" is displayed. In case that there is no error file, "a warning file" is displayed.

Break button

It is able to stop the "Pre-check for import" job.

When a file is prepared in the working folder the gray out of an icon is canceled. As EDIF reader creates LCDB template and circuit on the basis of these files,please edit(if necessary) it by clicking each icon after an "Pre-check for import" job is complete.

Although the editor is working to check the contents in "Library constitution table", please do not perform the editing. If error occurs in "Pre-check for import",please output EDIF file again with different setting and modifyby hand.

3.4 Import

When "Pre-check for import" is completed, please click a menu tab "Import".

To make LCDB template, please click the check box of "Generate a LCDB template". To make circuit and symbol library, please click the check box of "GenerateSymbol/Circuit sheet".

Scale (Please refer to chapter 2.3.1) is able to be adjusted on the occasion of transformation. "Unit inside an EDIF file" is multiplier. "Unit inside System Designer" is divisor.

There are three types of "Symbol Generation modes":

a. Create New

This mode creates a new symbol in the Library Name folder of the Work folder.

When creating a circuit diagram, this mode uses only newly created symbols to assemble the diagram.

b. Symbol Name and Pin Name Search

This mode searches for paths described in the symbol path table of the data resource, and if symbols with "the same symbol names and pin names are also all identical" are found, the symbol will not be generated. When creating a circuit diagram, this mode uses symbols that were searched by symbol name and pin name to assemble the diagram. If the pin locations of existing symbols or conversion scales are changed, connection to a net will no longer be possible.

c. Symbol Name Search

This mode searches for paths described in the symbol path table of the data resource, and if symbols with "the same symbol names" are found, the symbol will not be generated.

When creating a circuit diagram, this mode uses symbols that were searched by symbol name to assemble the diagram.

If the pin locations of existing symbols or conversion scales are changed, connection to a net will no longer be possible. Since searches are conducted by symbol name only, keep in mind that symbols may occasionally be selected unexpectedly.

Chapter 3 Operation

(1) Execute button

When "Execute" button is ON, EDIF reader starts to import and generate schematic data. In case that there is an error file when the Import is completed, "an error file" is displayed. In case that there is no error file, "a warning file" is displayed.

(2) Break button

It is able to stop the import job.

Chapter 4 Conversion rule outline

4.1 Files

The following files are generated by Import or pre-check.

(./ is Working folder)

files	file name	generate process
Data resource	./landata.rsc	Pre-check for import
Environment resource	./lanenv.rsc	Pre-check for import
Property conversion file	./propcnv.htb	Pre-check for import
Library constitution table	./precheck.htb	Pre-check for import
LCDB	./library name.prf	Import
	./library name.dbf	Import
	./library name.cmp	Import
	./library name.rlt	Import
Library folder	./library name folder	Import
Symbols	./library name folder/cellname.smb	Import
circuit folder	./library name folder/cellname.cir	Import
	+log,drc,frame,ext	
Schematic sheet	cellname.cir/page.sht	Import
Sheet net	ellname.cir/page.net	Import
Symbol list ^a	./symbolList.txt	Import
Sheet list ^a	./sheetList.txt	Import
LCDB list ^a	./lcdbList.txt	Import
error file	./edif2sd.err	Pre-check for import,Import
warning file	./edif2sd.wrn	Pre-check for import,Import

a. This file is generated for custom post-processing and not necessary for standard import.

4.2 Common item with all vendor

4.2.1 Property

The following item is default conversion rule. If property conversion file is customized and priority order is changed, you can follow it.

property name	Conversion rule
symbol file name	cell name
partName	cell name
cdbName	cell name
componentName	cell name + "_" + view name + "_" type(package or gate)
function	componentName
reference	designator
pin ID ^a	If designator is numeric, set designator to pin ID
	If designator is not numeric, reset pin ID in alphabet order
	If designator's text length is 0, reset pin ID in alphabet order
pinLabel	port name
pinNumber	designator in port
io property ^b	direction in port

- a. The conversion rules apply when the pin ID generation mode is specified as "auto."
Please refer to "5.2.5 pin ID generation mode" for how to map pin ID with specified properties.
- b. VCC and GND has special setting by each vendor name

4.2.2 Component Type

Component type(part,gate) is recognized by the constitution of cell.

View count	Pattern	Component Type
	no pins	figure
1	pinnumber is not multiple	parts
	pin number is multiple	gate
> 1	Pin numbers are same completely between view	parts(nega/posi)
	Between view pin number without doubling	multiple gate
	Part of pin number is doubling between	multiple gate view

Implied pin(The symbol without pin object such as a Power or Ground pin) is written in LCDB as a power supply box. (Symbol name is not set.)

4.2.3 Function Type

Function type is defined by the contents of designator in interface to the reference header letter of "Function Type Definition File" in System Designer. If the end of designator's string is "?" EDIF reader delete this before comparison.

For example
 (designator "R") ---> R
 (designator "R??") ---> R
 (designator "IC?") ---> IC

4.2.4 Bus label

property name	Setting rule
Symbol Path	Set as highest number of Symbol path with absolute path
Block Path	Set as highest number of Block path with absolute path
Parts Path	Set as highest number of Parts path with absolute path
Resource Path	Set Data resource,Environment resource path with Relative path

4.3 The items that have different processing by each vendor

4.3.1 Net label

The pattern of Array Net label

vendor name	Conversion rule
VIEWLOGIC	A[0:15] --> A[0-15]
	A[0:A/H] --> A[0-10]
	A[0:15:4] --> A[0],A[4],A[8],A[12]
MENTOR	A(0:15) --> A[0-15]

The netLabel of the net extracted from bus is renamed with bus name of its bit on the basis of the description of Ripper connection.

4.3.2 pin IO

Pin IO is only 3 kinds of "input" "output" "inout" on the agreement of EDIF, but in System designer, "VCC" and "GND" are necessary, so this is determined by the following pin property.

vendor name	Conversion rule
VIEWLOGIC	supplyType=power --> io=VCC
	supplyType=railGround --> io=GND
MENTOR	implicitPortClass:VCC --> io=VCC
	implicitPortClass:GND --> io=GND

4.3.3 Schematic sheet name

vendor name	Conversion rule
VIEWLOGIC	(page &10) --> 010.sht
MENTOR	(page sheet10) --> 010.sht

4.3.4 Offpage connector

There are no off page connector in VIEWLOGIC's EDIF file.

Although the symbol like off page connector is output as comment (commentGraphics) in VIEWLOGIC's EDIF version(7.5), this component has no information about pin or connection point, so, EDIF reader place it as a figure symbol.

4.4 The items that are peculiar generate LCDB

4.4.1 Equivalence

Equivalence can be transformed only in the pattern of simple pin exchange.

vendor name	Example of Conversion
VIEWLOGIC	In interface property (property PINSWAP (string"A,B")),if pin ID for A,B pin is A=1,B=2,equivalence becomes 1=2
VIEWLOGIC	From the interface property (property NC (string "A")), I/O of pin A is set to NC.

Chapter 5 Customizing

Operating the following files after performing "Pre-check for import" can customize transformation.

5.1 Data resource

5.1.1 Text table

As EDIF reader selects the nearest table number by text height, please define the tables of the various height.

5.2 Property conversion file

5.2.1 property name

Table name: properties

The "properties" table is used to transform EDIF 200 Schematic view property to System Designerproperty names.

One line consists of two fields, corresponding to one property name after conversion.

field number	Contents
1	property name in EDIF file
2	System Designer property name

A property name not defined in this table is transformed to System Designerdata with the property name defined in the property spec file.

Note that property names that are not registered in the property spec file cannot be viewed from the System Designereditor.

However, the following properties are first transformed internally to different property names and then transformed in priority order.

EDIF notation	Program internal name	Output property name
cell name	cellName	partName
designator in interface	cellDesignator	reference
port name	pinName	pinlabel
designator in port	pinIDesignator netName	pinNumber
net name	netName	netlabel

If (pinlabel,partName,reference,pinNumber) is specified in the property conversion table, the specification in the property conversion table has priority.

For example, the following specification gives priority to "DEVICE" over "Cell name (cellName)" , so "partName". is selected to transform.

Please make sure that the properties that are not registered in the property definition file (PropSpec) cannot be confirmed in the editor of System Designer.

```
properties{
  (DEVICE partName)
}
```

5.2.2 Property name unification flag

```
table name : letterNameType
```

As An English capital letter and small letter sometimes co-exist in EDIF file, this flag unifies property name either capital or small letter (Because those are sometimes regarded as same property in other company system)

Yet, the property name that has been registered in the table "properties" is out of unification.

Key word	Function
capital	capital character is specified
small	small character is specified
free	no specification

```
letterNameType : capital
```

Above example, capital character is specified.

Yet, the following system reservation property names are not unified.

Alias	property name
Part Name	partName
CDB Name	cdbName
Component Name	componentName
Function Name	function
Reference Designator	reference
Block File Name	blockName
Circuit Path Number	circuitPathNo
Component Type in symbol file	componentType
Function Type in symbol file	functionType
Net/Bus Label	net Label
Global FFlag	global
Pin Label	pin Label
Pin Number	pinNumber
IO	io
pinType	pinType
Common Terminal?	isCommonTerminal

5.2.3 property value

table name: propertyValue

When it needs to change a part of a property value to a different character, this filter is used.

field number	Contents
1	Text in EDIF file
2	Text in System Designer
3and more	Filtering property name

```

For example)
propertyValue{
  (" " "_" netLabel partName pinLabel )
  ("m" "M" value )
  ("k" "K" value )
  ("u" "U" value )
  ("X" "x" value partName pinLabel )
}
    
```

5.2.4 Property value unification flag

table name: letterValueType

This is used to unify English character of the property value when property value has to be English capital character (For example, when CR-5000/PWS is used for layout system).

Yet, please do not use it as much as possible, because a net sometimes can not be connected normally.

Key word	Function
capital	capital character is specified
small	small character is specified
free	no specification

The property name that has been registered in the table (propertyValue) is out of unification.

letterValueType : free

Above example, character is not unified.

5.2.5 Pin ID Generation Mode and Pin ID Generation Method

table name:pinIDGenerateMode

This is used to control how to decide the pin ID based on the property of port (pin) described in EDIF.

Key Word	Contents
auto	Assigns the designator as a key (Refer to [4.2.1 Each property]).
property	Specifies the name of the property that is assigned to the port which is used assign the pin ID.

table name:pinIDPropertyMethod

Defines how to deal with the value of the property specified for "pinIDGenerateMode".

If "pinIDGenerateMode="auto" is set, then it is not referred to.

Key Word	Contents
value	The property value will be used as the pin ID. In this case the property value must be an integer greater than 1.
sort	The property values are "sorted by schematic symbol", then they will be generated starting from number 1.

The following samples show the property value for pin property, "LOG_PIN_NO" is used as Pin ID.

Example: pinIDGenerateMode : LONG_PIN_NO
pinIDPropertyMethod : value

5.2.6 LCDB Link Mode

table name:pinIDPropertyMethod

In the Generate Schematic/Symbol Library, you can specify whether CDB names and component names, which are generated in the Generation of LCDB template, are applied to the schematic data .

If you want to only import the symbol library and make a separate LCDB, specify "NO" in this case.

Key Word	Contents
yes	A CDB name and the component names are applied.
not	A CDB name and the component names are not applied.

5.2.7 File name

table name:fileChar

The "fileChar" table is used to replace characters used for file (symbol file/circuit folder name/block file name) created by the EDIF reader.

You can set this if special character is included in cell name or library name of EDIF file and the creation of symbol file cause the contravention of system restriction.

Please use this table as a filter if a file that cannot be used in UNIX or MS-DOS is created.

field number	Contents
1	one text in cell name or library name
2	one text in file name after conversion

The following character is set up as default. (Please do not delete unnecessarily as there is a possibility that transformation cannot be performed.)

```

fileChar{
  ( "." " _" )
  ( "!" " _" )
  ( "####" " _" )
  ( "$" " _" )
  ( "%" " _" )
  ( "&" " _" )
  ( "" " _" )
  ( "(" " _" )
  ( ")" " _" )
  ( "*" " _" )
  ( "+" " _" )
  ( "-" " _" )
  ( "/" " _" )
  ( "." " _" )
  ( "<" " _" )
  ( ">" " _" )
  ( "?" " _" )
  ( "[" " _" )
  ( "####" " _" )
  ( "]" " _" )
  ( "^" " _" )
  ( "" " _" )
  ( "_" " _" )
  ( "" " _" )
  ( "" " _" )
}

```

5.2.8 Power/Ground Mode

Table Name : vccgndMode

When supplyType is set for the power / ground cell, that cell is recognized as the power / ground and is converted to SD.

The default is "no".

Keyword	Contents
yes	Recognizes the power / ground.
no	Does not recognize the power / ground.

5.2.9 Ripper Mode

Table Name : ripperMode

This mode is employed when rippers are used for complex ripper configurations or when rippers are not used for bus and net connections in EDIF. Buses and nets can be connected by specifying "no" when rippers are not used. Specify "intelligent" when complex configurations of rippers are used in EDIF. However, extremely complex ripper configurations may not be properly converted.

Keyword	Contents
no	Setting for bus and net connections not using rippers
intelligent	Setting for complex ripper connections

5.2.10 Line Width

Table Name : pathWidthMode

Select the closest line width from the line width table in the data resource file. When "no" is selected, table number 0 is used while only buses use number 1. The initial number is "no" by default.

Keyword	Contents
yes	Changes the line width.
no	Does not change the line width.

5.3 Library constitution table

The property name described in cell or port inside EDIF is written in this file and "LCDB parameter" file is created based on this. So the property that doesn't have to be written in LCDB can be adjusted by deleting the property name of this file.

```

For example)
test LIB{
  ( MAXVIEWCOUNT 2 )
  ( CMP "@CP" "@CS" "@LS" "@RS" "ALT" "CADCAT" )
  ( CMP "GLOBAL" "HETERO" "LABEL" "LEVEL" "MODEL" )
  ( PIN "CPU_SRESET" "GPI011" "PINTYPE" "SWAP" )
  ( CELL "gn-arhin" 1 )
  ( CELL "gn-gndlb" 1 )
  .....
}

```

Above example "test_LIB" is a library name. Please do not change it.

The contents of the table are as follows.

Keyword	Contents	Changeable or not
MAXVIEWCOUNT	Max view count in a library	not changeable
CMP	property name in interface	removable
PIN	property name in port	removable
CELL	cell name and cell constitution type number ,Scale adjustment value	not changeable

Chapter 6 Limitations

6.1 Limitations from EDIF syntax

(1) Power and Ground symbols

The component that should be the POWER/GROUND in System Designer is transformed as a hierarchy connector. It is because that the information that distinguishes a hierarchy connector and the POWER/GROUND in the EDIF file is lacking. Editing by hand necessary after transformation.

(2) instance block property

When multiple same circuit blocks are used and property values in the block have different design, it cannot be transformed by EDIF.

(3) Text height

In EDIF, only the text height information can be transformed.

The information about text width and space cannot be transformed.

6.2 Limitations from System Designer

- (1) Color
The default value specified in the data resource for conversion is used as the color for each object.
- (2) Line type
EDIF reader is using the table number 0 in Data resource, because System designer can not change the pattern of short dash line freely.
- (3) Hatching
Hatching pattern of polygon is always using table number 1.
- (4) Joined in Ripper symbol
This program supports ripper symbols that have two terminals (multiple pins), and pin number for one terminal is same.
Rippers with two cross-connected pins are not supported.
- (5) Multiple Expressions
EDIF reader transforms range notation characters showing multiple expressions, but it does not cover the complicated specification of each vendor. Multiple expressions that can be read with in this program follows the way of the notation of the CR-5000/System Designer.
- (6) Pins on schematic sheet
System Designer does not place pins on a schematic sheet. Pins are generated on a schematic sheet and data for connecting nets are generated after being replaced with connector symbol pins.
- (7) Negative logic expression characters
This program does not transform negative logic expression characters. For circuits in which negative logic expression characters are used for signal names or pin names, set the negative logic expression characters used by each vendor system in (nlogicStartChar, nlogicEndChar) of the data resource.
- (8) Variable net label and frame
Variable repetition expression (frame and net in MENTOR EDIF) is not able to transform.