

**Software**  
**New Functions Reference Manual**

CR-5000 Board Designer

Rev. 6.0

## PREFACE

This manual outlines additions and improvements to the functions of the CR-5000 Rev. 6.0. It also contains information about optional software.

For more information on the individual functions and operation, see the “User's Guide” or the “online help” for each tool.

*If you have any questions, call*

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## Notation

The following abbreviations represent the products in the table below unless otherwise stated.

### <Abbreviation and product>

Abbreviation	Product
SD	System Designer
CDB	Components Manager or the whole component library
BD	Board Designer
BP	Board Producer

The table below lists paths that the environmental variables in this manual indicate.

### <Environmental variable and path>

Environmental variable	Path indicated by environmental variable
\$ZLOCALROOT	(CR-5000 installation directory)/local
\$ZSYSROOT	(CR-5000 installation directory)/zsys
\$ZUEROOT	(CR-5000 installation directory)/zue
\$ZCSROOT	(CR-5000 installation directory)/zcs
\$ZDSROOT	(CR-5000 installation directory)/zds
\$ZPLSROOT	(CR-5000 installation directory)/zpls
\$ZPMSROOT	(CR-5000 installation directory)/zpms

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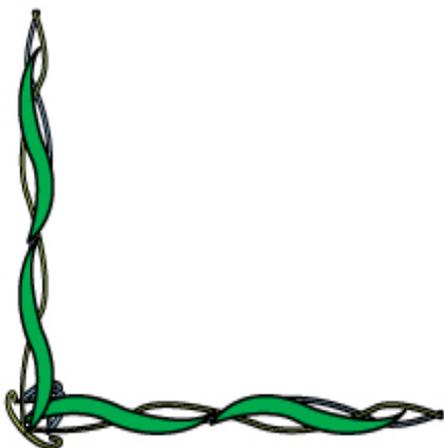
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# **Chapter 1**

## **Common to CR-5000**



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# 1-1 Converting Databases from Rev. 5.0 to Rev. 6.0

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The following object-oriented databases created using Rev. 5.0 must be converted to Rev. 6.0 database. You can convert the database in two ways: command execution and automatic execution.

- Execution using the Database Conversion Program (zdbevolv)
- Automatic execution

## <Database that should be converted>

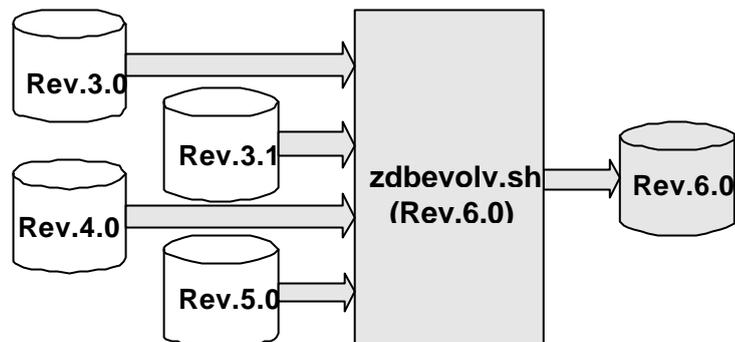
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•Design rule library	XX.rul						
•Manufacturing rule library	XX.mrdb						
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•PCB database	XX.pcb						
•Design rule database	XX.rul						
Manufacturing panel database	<table border="1"><tr><td>•Panel database</td><td>XX.pnl</td></tr><tr><td>•Manufacturing rule database</td><td>XX.mrl</td></tr></table>	•Panel database	XX.pnl	•Manufacturing rule database	XX.mrl		
•Panel database	XX.pnl						
•Manufacturing rule database	XX.mrl						

## ● Execution using the Database Conversion Program (zdbevolv)

### [Function]

The Database Conversion Program (zdbevolv) converts the object-oriented database file created using Rev. 5.0 to Rev. 6.0 database file.

This program can also convert the object-oriented database file created using Rev. 3.0, Rev. 3.1 or Rev. 4.0 directly to Rev. 6.0 database file.



### <Convertible file version and type>

File type	File version			
	Rev. 3.0	Rev. 3.1	Rev. 4.0	Rev. 5.0
Part library (prt)	C			U
Package library (pkg)	C			U
Footprint library (ftp)	C			C
Technology library (tch)	C			U
Design rule library (rul)	NC	C		C
Manufacturing rule library (mrdb)	NC	C		C
PCB database (pcb)	NC	C	C	C
Design rule database (rul)	NC	C		C
Panel database (pnl)	NC	C	C	C
Manufacturing rule database (mrl)	NC	C		C

C: Convertible

N: Not convertible

U: Unnecessary

## [Operation]

To start the Database Conversion Program (zdbevoldv), enter the following.

**zdbevoldv.sh    Required parameter    [Optional parameter]**

\* On the Windows-version, use zdbevoldv.exe for activation.

### 1. Required parameter

#### **Filename or directory (folder) name**

Filename or directory (folder) name of database to be converted. To specify multiple names, delimit them with a space.

### 2. Optional parameters

#### **-m recursive**

Upgrades sub-directories in the specified directory as well. This is valid only when a directory name is specified for execution.

#### **-m nobackup**

Upgrades files without creating save file.

<Example> To use a PCB file “ex,” which has been created using Rev. 5.0, with Rev. 6.0

**zdbevolv.sh ex** **Return**

In the above example, “ex.pcb” and “ex.rul” in the current directory are converted to Rev. 6.0 databases and the previous versions are stored as the save file under different names.

### [Notes and Restrictions]

- The program reserves a temporary saves you the time and work in area for upgrading in a target database file when upgrading a database file of Rev. 4.0 or older. Therefore, the file size may increase by about 1.5 times after upgrading.

### Reference

For execution from the File Manager, see “1-7 Design File Manager Schema evolution (Database Conversion Program).”

## ● Automatic execution

### [Function]

If the following environment variable is set, the CR-5000 system automatically upgrades a file created on a previous version when opening it for editing. In this case, a save file is not created.

```
ZCRDB_VERSIONUP =Auto
```

### [Notes and Restrictions]

- If forward annotation is executed in the automatic upgrading environment, for example, each CDB library is upgraded when the file is accessed. Be careful if you want to maintain the previous version files.
- This environmental variable is valid only for Rev. 5.0 database files.  
To upgrade databases created using Rev. 4.0 or an older version, use the Database Conversion Program (zdbevolv).

---

# 1-2 Converting Databases from Rev. 6.0 to Rev. 5.0

---

## [Function]

The following object-oriented databases edited using Rev. 6.0 must be converted to the Rev. 5.0 database to open them on the CR-5000 system Rev. 5.0.

Library database	<ul style="list-style-type: none"><li>•Footprint library XX.ftp</li><li>•Design rule library XX.rul</li><li>•Manufacturing rule library XX.mrdb</li></ul>
PC board design database	<ul style="list-style-type: none"><li>•PCB database XX.pcb</li><li>•Design rule database XX.rul</li></ul>
Manufacturing panel database	<ul style="list-style-type: none"><li>•Panel database XX.pnl</li><li>•Manufacturing rule database XX.mrl</li></ul>

These databases may contain attributes that can be set only with Rev. 6.0. zdb6to5.sh detects such attributes, outputs warning messages, and changes or deletes them to make the databases editable with Rev. 5.0. The attributes to be changed or deleted are listed in **[List of attributes to be processed]**.

## [Operation]

To start the Database Conversion Program (zdb6to5), enter the following.

```
zdb6to5.sh Required parameter [Optional parameter]
```

\* On the Windows-version, use zdb6to5.exe for activation.

### Required parameter

**Filename or directory (folder) name**

Filename or directory (folder) name of database to be converted.

<Example> To use a PCB file “ex,” which has been edited using Rev. 6.0, with Rev. 5.0.

```
zdb6to5.sh ex Return
```

In the above example, “ex.pcb” and “ex.rul” in the current directory are converted to Rev. 5.0 databases and the current versions are stored as the save file under different names.

## Reference

For details on operations, see “CR-5000 User’s Guide/5.7.6 Downgrading the files”.

## [List of attributes to be processed]

### Footprint library

Data	Attribute	Process
Round hole, oblong hole, padstack	Hole type	The hole-type range on the previous version is 0 to 15. If 16 or higher is set, the range defaults to 0..
Related to character dimension line	User font	The user font cannot be used on the previous version. This is changed to System Font 'zafont.'
Characters on the conductive layer		On the previous version, character input was prohibited on a layer if the layer type in the footprint is conductive. This attribute is deleted.

### Design rule library

Data	Attribute	Process
Board specifications	Mesh plane cutout figure limit	This information was not settable on the previous version, so this is deleted.

### Manufacturing rule library

Data	Attribute	Process
Tool	Hole type	The hole-type range on the previous version is from 0 to 15. If 16 or higher is set, the range defaults to 0.

### PCB database

Data	Attribute	Process
Round hole, oblong hole, padstack	Hole type	The hole-type range on the previous version is from 0 to 15. If 16 or higher is set, 0 is set.
Pad, padstack	Trimming probe	The trimming probe attribute cannot be set on the previous version. This is changed to normal pad or padstack.
Padstack	Plating attribute	Wiring keep-out attribute Not to be processed. Note that the following processing results may be different because the previous version does not support the plating attribute. (1) Non-connected net calculation/net extraction (Only the plating attribute is affected) (2) Automatic change to land status (3) Land status and figure cutout on surface input (4) Processing related to wiring editing such as line leading on wiring input (5) Error determination with DRC For details, see "Board Designer User's Guide, Vol.2/4.9, Treatment of Padstack Plating Attribute."
Component	Real number angle	Only an integer can be set as component angle on the previous version. A real number is replaced with the integer calculated by rounding off the first decimal point. Shapes in the component are rewritten according

		to the new component angle.
Related to character dimension line	User font	The user font cannot be used on the previous version. This is changed to System Font 'zafont.'
Wiring line	Pen shape	On the previous version, the pen shape for the wiring line should be circular. A square pen shape is changed to circular.
Character on the layer of which type in the footprint is conductive		On the previous version, character input on a layer is prohibited if the layer type in the footprint is conductive, so this attribute is deleted.
Shield surface data		The shield attribute cannot be set for surface data on the previous version. Such data is rewritten to normal surface data.

### Design rule database

Data	Attribute	Process
Board specifications	Mesh plane cutout figure limit	This information was not settable on the previous version, so this attribute is deleted.
Pin pair group	Maximum and minimum wiring length rule	This information was not settable on the previous version, so this attribute is deleted.
Electrical net		This information was not settable on the previous version, so this attribute is deleted.

### Panel database

Data	Attribute	Process
Round hole, oblong hole, padstack	Hole type	The hole-type range on the previous version is from 0 to 15. If 16 or higher is set, the range defaults to 0.
Component	Real number angle	Only an integer can be set as component angle on the previous version. A real number is replaced with the integer calculated by rounding off the first decimal point. Shapes in the component are rewritten according to the new component angle.
Related to character dimension line	User font	The user font cannot be used on the previous version. This is changed to System Font 'zafont.'
Character on the layer of which type in the footprint is the conductive layer		On the previous version, character input on the layer is prohibited if the layer type in the footprint is conductive. This attribute is deleted.

### Manufacturing rule database

Data	Attribute	Process
Tool	Hole type	The hole-type range on the previous version is from 0 to 15. If 16 or higher is set, the range defaults to 0.

---

# 1-3 Operation with Different System Designer Versions

---

With Rev. 5.0 or later, you can operate the System Designer (hereafter, SD) and the Board Designer (hereafter, BD) even if they are different versions.

However, you cannot transmit attributes added with an upper version to a lower version.

Before using different versions, read through the following restrictions.

- Mixing versions
  - Using the SD 5.0xx and BD 6.0xx
  - Using the SD 6.0xx and BD 5.0xx
- \* 5.0xx indicates all sub-versions of Rev. 5.0.  
\* 6.0xx indicates all sub-versions of Rev. 6.0.

## ● Mixing versions

### [Function]

You can install the SD and BD in the same node and operate them even if one of them is Rev. 5.0 and the another is Rev. 6.0.

### [Operation]

When building an environment for different versions, install Rev. 5.0 before Rev. 6.0.

### [Notes and Restrictions]

- Although the File Managers for the SD and BD are integrated, the start icon display is determined by license. Because the File Manager for Rev. 6.0 is started, the Rev. 5.0 license can not be referred to and icons for Rev. 5.0 tools are shaded (grayed) and unavailable.

To start a Rev. 5.0 tool, display the Assist Menu by right-clicking and then start the tool.



- Notes on the Windows version only

The Plotting Environment Setup Tool uses Rev. 6.0 tools when different versions exist.

Start the Plotting Environment Setup Tool from the Rev. 6.0 menu.

## ● Using the SD 5.0xx and BD 6.0xx

### [Notes and Restrictions]

The following restrictions on using the SD 5.0xx and BD 6.0xx exist.

- Cross-probing
- Forward and back annotation
- Setting the plotting environment (for Windows version only)

### **Cross-probing**

You cannot group components from the SD.

### **Forward and back annotation**

If the following attributes are set on the BD, they are not reflected to the schematic.

If forward annotation is performed in this case, BD-set values are deleted.

[Net rule]

- Pair net name
- Maximum parallel wiring length for crosstalk check
- Specification prohibiting grounding
- Maximum wiring capacity

[Component rule]

- Constant
- Reference fixing flag

### **Setting the plotting environment (for Windows-version only)**

Start the tool by selecting [CR-5000 PCB layout system] [Utility] [Plotter Setting] from the start menu.

## ● Using the SD 6.0xx and BD 5.0xx

### [Notes and Restrictions]

The following restrictions on using the SD 6.0xx and BD 5.0xx exist.

- Cross-probing
- Forward annotation restriction
- Restriction on creating net groups
- Note on setting the plotting environment (for Windows version only)

### **Cross-probing**

You cannot group components from the SD.

### **Forward annotation restriction**

If the following attributes or rules are set on the SD, an error occurs ending the process at forward annotation.

[Net rule (Sheet Editor)]

- Maximum parallel wiring length for crosstalk check

[Electrical net rule (Electrical Net Editor)]

- Maximum wiring length
- Minimum wiring length

[Topology rule (Topology Design Tool)]

- Via rule
- Pin pair rule: maximum and minimum wiring widths
- Pin pair group rule: maximum and minimum wiring lengths

### **Restriction on creating net groups**

You cannot create net groups using the Electrical Net Editor.

To create a net group, edit the file below and set the “net group” value with the Attribute Change dialog box for the Sheet Editor as with the SD Rev. 5.0.

[\$ZDSROOT/etc/{jpn,eng}/PropSpec]

The same two lines as shown below in the file appear. Delete the comment declaration characters (#) on the two lines.

```
# (netGroup text “net group” ON - 1)
```

```
(netGroup text “net group” ON - 1)
```

[\$ZDSROOT/etc/cr5ruf.frm]

Just as with net group operation for Rev. 5.0, use cr5ruf3.frm as the format file for outputting the design rule list.

If Format File \$ZDSROOT/etc/cr5ruf.frm is referred to, copy \$ZDSROOT/etc/cr5ruf3.frm to cr5ruf.frm.

### **Note on setting the plotting environment (for Windows-version only)**

Start the Tool by selecting [CR-5000 System Designer 6.0] [Utility] [Plotter Setting].

# 1-4 List of Changed Resource Files

Resource file name	Changed
\$ZCSROOT/info/cdb.rsc	Yes
\$ZCSROOT/info/part.rsc	Yes
\$ZCSROOT/info/pinassign.rsc	Yes
\$ZCSROOT/info/function.rsc	Yes
\$ZCSROOT/info/package.rsc	Yes
\$ZCSROOT/info/footprint.rsc	Yes
\$ZCSROOT/info/padstack.rsc	Yes
\$ZCSROOT/info/pad.rsc	Yes
\$ZCSROOT/info/dispdbk.rsc	No
\$ZCSROOT/info/cdbabst.rsc	Yes
\$ZCSROOT/info/databook.rsc	New
\$ZCSROOT/info/jpn(eng)/dimrules.dbt	Yes
\$ZCSROOT/info/jpn(eng)/search.rsc	Yes
\$ZCSROOT/info/jpn(eng)/databook.dbt	Yes
\$ZCSROOT/info/jpn(eng)/figure.rsc	Yes
\$ZCSROOT/info/jpn(eng)/apptypes.cmm	Yes
\$ZUEROOT/info/board.rsc	Yes
\$ZUEROOT/info/library.rsc	No
\$ZUEROOT/info/propdefs.rsc	Yes
\$ZUEROOT/info/tpprobe.rsc	New
\$ZUEROOT/info/jpn(eng)/zfilemgr.rsc	Yes (deleted)
\$ZUEROOT/info/jpn(eng)/zfmcustm.rsc	Yes (deleted)
\$ZPLSROOT/info/custom/cmacro.rsc	No
\$ZPMSROOT/info/custom/cmacro.rsc	No
\$ZSYSROOT/info/dbparam.rsc	No
\$ZLOCALROOT/zsys/info/zui.rsc	Yes
\$ZLOCALROOT/zsys/info/jpn(eng)/zfilemgr.rsc	New
\$ZLOCALROOT/zsys/info/jpn(eng)/zfmcustm.rsc	New
\$ZUEROOT/info/parameter.rsc	Yes
Plotter-related file	Yes

## ● Using resource files

Items in the tool and data resource files for each tool are added or changed in line with the upgrade to Rev. 6.0.

Before using a Rev. 5.0 resource file on Rev. 6.0, check changes to each resource file.

Rules for installing resource files are as follows:

### Type (1)

This type of resource file can be used with Rev. 6.0 without modification.

Leave the existing Rev. 5.0 resource file unchanged and install the Rev. 6.0 resource file by adding extension “.new.”

Example      **cdhabst.rsc**      **cdhabst.rsc.new**

Existing resource      File for Rev. 6.0  
file (for Rev. 5.0)

### Type (2)

The type of resource file cannot be used as is with Rev. 6.0.

Add extension “.bk” to Rev. 5.0 resource files and install Rev. 6.0 resource files.

Example      **sample.mrdh**      **sample.mrdh.bk**

File for Rev. 6.0      Existing resource  
file (for Rev. 5.0)

### Type (3)

This type of resource file is not available to the public and is overwritten upon upgrading.

### Type (4)

This is the secret resource file that tools no longer refer to after upgrading. Nothing is done upon upgrading.

The attribute items of Part, StockID, PartTerm, GateTerm, Package, Footprint, Pinassign and Padstack are added, changed or deleted. Although you can use a resource file of Rev. 5.0 or older as is, you cannot set a value for attribute items newly added for Rev. 6.0 with Components Manager GUI.

**<Part\*Property parameter added>**

Parameter	Detailed explanation
EnetNonSeries	<p>Component non-series attribute for electrical net evaluation. Normally, the nets connected to both pins of a 2-pin component are regarded as the same electrical net on electrical net evaluation.</p> <p>You may not want to regard such connected nets as the same electrical net (for example, the terminal resistor for differential signals). In this case, specify "YES."</p> <p>YES : The nets connected to both pins of a 2-pin component or 2-pin function are not regarded as the same electrical net.</p> <p>No setting or other than "YES" : The nets connected to both pins of a 2-pin component or 2-pin function are regarded as the same electrical net.</p>
PrintedPartType	<p>Printed resistor attribute.</p> <p>"resistor" or nothing is set to this attribute.</p> <p>"resistor" indicates a printed resistor.</p> <p>* Even if a part attribute is not set to [Printed component], the part is regarded as a printed resistor if this attribute is set.</p> <p>resistor : Indicates that the object is a printed resistor.</p>
PlacementLayer	<p>Placement side limit attribute.</p> <p>When you try to place a reference component on the side not specified with the attribute, a Component DRC error occurs.</p> <p>A : Placement possible on the A-side only</p> <p>B : Placement possible on the B-side only</p> <p>Both : Placement possible on both sides</p> <p>Neither : Placement impossible on both sides</p> <p>This attribute can be set for footprints.</p> <p>* The reference priority is part footprint.</p>
PlacementAngle	<p>Placement angle limit.</p> <p>If a reference component is outside of the specified placement angle, a Component DRC error occurs. The angle is specified in 45° units.</p> <p>All : All angles possible</p> <p>x:y:z... : angles in x,y,z can be specified</p>

elec_type	<p>For Hot-Stage.          Defines the 2-pin component types used on Hot-Stage such as capacitor, resistor and inductor. Character string type.</p> <p>cap : Capacitor          res : Resistor          ind : Inductor          dio : Diode          Others : The specified value is transmitted to Hot-Stage.</p>
hs_value	<p>For Hot-Stage.          Defines the 2-pin component type used on Hot-Stage. Character string type.</p> <p>capacitor : pF          resistor : ohm          inductor : nH</p> <p>(Note) Although you can write units, Hot-Stage ignores data other than numbers.          (Note) Be sure to always set 0 for diode.</p>
hs_model	<p>For Hot-Stage.          Transmission line model name used on Hot-Stage. Character string type.</p>
emcPart	<p>emcPart setting</p> <p>YES : Specified to regard the object as EMC part.          NO : Specified not to regard the object as EMC part.</p>

**<Part\*Property parameter deleted>**

Parameter	Detailed explanation
blockName	Deleted due to change to the SD specifications.
EMCPart	Deleted due to change to parameter name. (New name: emcPart)

**<Stock ID \*Property parameter added>**

Parameter	Detailed explanation
compAreaBtmHeight	<p>Defines the minimum height for component area input in the footprint. This can be assigned to the stock code and component attributes and referred to in that order. When this is omitted, the height defined with the package attribute or the component height defined in the footprint is applied. The unit is in millimeters.</p>
compAreaTopHeight	<p>Defines the maximum height for component area input in the footprint. This can be assigned to the stock code and component attributes and referred to in that order. When this is omitted, the height defined with the package attribute or the component height defined in the footprint is applied. The unit is in millimeters.</p>

**<PartTerm\*Property and GateTerm\*Property parameter added>**

Parameter	Detailed explanation
enetSeries	Assigned to pins targeted by electrical net evaluation. Multiple nets connected to the pins in the same component and with the same "enetSeries" attribute are regarded as the same electrical net.
tthl	For Hot-Stage. Falling transit time (driving time) used on Hot-Stage. Character string type. If the unit is omitted, default is ps. You can specify ns as unit.
tthh	For Hot-Stage. Rising transit time (driving time) used on Hot-Stage. Character string type. If the unit is omitted, default is ps. You can specify ns as unit.
voh	For Hot-Stage. High-level output voltage used on Hot-Stage. Floating point type. The unit is in V.
vol	For Hot-Stage. Low-level output voltage used on Hot-Stage. Floating point type. The unit is in V.
cpin	For Hot-Stage. Pin capacity used on Hot-Stage. Character string type. If the unit is omitted, default is pF. You can specify a unit.

**<Package\*Property parameter added>**

Parameter	Detailed explanation
compDRCGroup	Component DRC group name. You can set clearance per component with design rules using group name as key. Component DRC is executed according to the rule set specified on the BD.

**<Footprint\*Property parameter added>**

Parameter	Detailed explanation
ignoreLayoutArea	Specifies to ignore board edge during DRC. When this parameter is set to YES in the footprint, the component referring to the footprint does not cause an error even if it overlaps a layout area on the BD, (valid during Area DRC and Component DRC).
placementLayer	Limits the placement side. When you try to place a reference component on the side not specified with this attribute, a Component DRC error occurs. A : Placement possible on the A-side only B : Placement possible on the B-side only Both : Placement possible on both sides Neither : Placement impossible on both sides This attribute can be set for parts. * The reference priority for reference is part footprint.

placementAngle	Limits placement angle. If a reference component is outside of the specified placement angle, a Component DRC error occurs. The angle is specified by 45° unit. All : All angles possible x:y:z... :angles in x,y,z can be specified
scaling	Specifies permission to scale a component not on the schematic for the component input command of the Artwork or Panel Tool. YES : Component scaling permitted NO : Component scaling prohibited (Values other than “NO (in upper-case characters)” are regarded as “YES.”)
placeLayerNo	Used for identification as an inner-layer component and specifies a layer on which the inner-layer component is placed. Indicates to what layer the footprint belongs. Layer Number 0 indicates that the object is an inner-layer component and the layer this object belongs to is not recognized. When the specified inner layer number is not within the inner layer range, the specification is invalid. The valid range inside the layer number is as follows: For Layer N (N>=3), (2 <=Inner layer number <=N - 1)

**<Pinassign\*Property parameter deleted>**

Parameter	Detailed explanation
blockName	Deleted due to change to the SD specifications.

**<Padstack\*Property parameter added>**

Parameter	Detailed explanation
noWiring	Prohibits wiring. The Placement/Wiring Tool cannot perform wiring retraction, extension and net connection for the padstack with this attribute. As well, the padstack is not connected to a line, surface or other objects. If clearance to such a figure is not sufficient, a DRC error occurs. (This attribute is commented out on installation.) YES : Wiring prohibited. If the parameter is omitted or any value is not set, wiring is possible. All input attributes are regarded as YES.

- **\$ZCSROOT/info/part.rsc** **Type (1)**
- **\$ZCSROOT/info/pinassign.rsc** **Type (1)**
- **\$ZCSROOT/info/function.rsc** **Type (1)**
- **\$ZCSROOT/info/package.rsc** **Type (1)**

One parameter is added.

Although you can use these Rev. 5.0 resource files as they are, note that “default” is set to parameters newly added for Rev. 6.0.

**<Added item>**

Parameter	Detailed explanation	Default
ConfirmMode	Specifies whether to display a dialog box to confirm saving. ON : Displays the dialog box. OFF : Does not display the dialog box.	OFF

- **\$ZCSROOT/info/footprint.rsc** **Type (1)**

35 parameters are added, 3 parameters are changed, and two parameters are deleted. Although you can use this Rev. 5.0 resource file as is, note that “default” is set to parameters newly added for Rev. 6.0.

**<footprint.rsc parameter added>**

Parameter	Detailed explanation	Default
gridTable	Defines combination of grid information (grid name, X-direction pitch, Y-direction pitch) that can be selected to specify a grid pitch.	None
textSizeTable	Defines combination of character size information (character width, character height, character interval and pen width) and identification name that can be selected to specify a character size.	None
penWidthTable	Defines values to specify the pen width for a line, surface and character.	None
fontName_Motif	Font name for displaying the pin number, cursor coordinates and ruler on the UNIX-version.	“variable”
fontName_MSwindows	Font name for displaying the pin number, cursor coordinates and ruler on the Windows version.	“Lucida Console/18 /Normal”
trapSize	Specifies a search trap side in pixels. Specify 1 or larger integer.	10
ConfirmMode	Specifies to display a dialog box to confirm saving. ON : Displays the dialog box. OFF : Does not display the dialog box.	OFF

offsetLineBasePos	Base position used when generating a figure from a line using the offset figure input command. Edge : Outline Center : Center locus	Edge
offsetDeleteBaseFigure	Specifies whether to delete reference figures using the offset figure input command. ON : Deletes. OFF : Does not delete.	OFF
subCanvas	Maximum number of sub-canvases to display. Specify an integer between 1 and 5.	3
pinNoJustify	Specifies whether to display the pin number and the reference point to display characters. OFF : Does not display LowerLeft : Lower left LowerCenter : Lower center LowerRight : Lower right MiddleLeft : Middle left MiddleCenter : Center MiddleRight : Middle right UpperLeft : Upper left UpperCenter : Upper center UpperRight : Upper right	LowerLeft
viewCoord	Specifies whether to display cursor coordinates on the canvas. ON : Displays. OFF : Does not display.	ON
coordPosition	Display position for cursor coordinates on the canvas. Cursor : Tracks the cursor. Fix : Fixed on lower right of the canvas.	Cursor
zoomRatio	Zoom ratio. Specify an integer between 5 and 100.	25
panRatioX	Panning ratio in the X-axis direction. Specify an integer between 5 and 100.	50
panRatioY	Panning ratio in the Y-axis direction. Specify an integer between 5 and 100.	50
requestDetail	Specifies the detail mode for the Query Data command. true : Detail mode false : Simple mode	true
ruler	Specifies whether to perform the minimum distance (ruler) display using the Change Shape Attributes command or Query Data command. ON : Displays. OFF : Does not display.	ON
rulerHeight	Graduated ruler height. Specify a real number (the unit set to unitType is used).	0.1

RulerPitch	Ruler pitch. Specify a real number (the unit set to unitType is used).	0.1
rulerDataSearch	Specifies whether to search data when specifying coordinates with the ruler command. ON : Searches data. OFF : Does not search data.	OFF
rulerXYDistance	Specifies whether to display distances in X- and Yaxis directions when displaying the ruler. ON : Displays. OFF : Does not display.	OFF
tangentArcMode	Automatic tangent arc mode on line, surface (window) and area input. ON : Sets automatic tangent arcs. OFF : Does not set automatic tangent arcs.	OFF
dimTarget	Specifies the reference point for length dimension line. Construct : Vertex Nearest : The nearest point	Construct
dimLeaderType	Specifies a leading line type. Leader : leader Balloon : balloon LeaderText : leader text	Leader
dimArrowDirect	Specifies the arrow direction for dimension line. Inside : To inside Outside : To outside	Inside
dimLeaderArrowShape	Specifies an arrow shape for text leading line. None : None. Dot : (dot) JIS : JIS ANSI : ANSI	ANSI
dimTextOffset	Dimension text offset from dimension line. Specify a real number (the unit set to unitType is used).	0.0
dimLinearValueType	“UserDefined” is added to the existing keywords.	Length
dimRadiusValueType	“UserDefined” is added to the existing keywords.	Diameter
dimAngleValueType	“UserDefined” is added to the existing keywords.	Degree
dimLeaderValueType	“UserDefined/Auto” is added to the existing keywords.	Diameter
dimTextJustify	“LowerLeft/LowerRight/MiddleLeft/MiddleRight/UpperLeft/UpperCenter/UpperRight” are added to the existing keywords.	LowerCenter
dimLeaderAngle	“Free” is added to the existing keywords.	60
dimRadiusAngle	“Free” is added to the existing keywords.	0

**<footprint.rsc parameter changed>**

Parameter	Detailed explanation
TermsNameTable	The format is expanded and a comment is added to the file.
DIP	Expanded to specify a padstack name for the corner pin for parametric registration [DIP/SOP].
PGA	Expanded to specify the number of pins for the center ball each in the X- and Y- directions for parametric registration [PGA].

**<footprint.rsc parameter deleted>**

Parameter	Detailed explanation
fontName	Deleted because fontName_Motif and fontName_MSwindows are newly set. However, if fontName_Motif is not specified on the UNIX version or fontName_MSwindows is not specified on the Windows version, the value set to this keyword is valid.
searchTrap	Deleted because the way to specify the length of a search trap side is unified with board.rsc. Use trapSize instead.

**● \$ZCSROOT/info/padstack.rsc**

**Type (1)**

Three parameters are added.

Although you can use this Rev. 5.0 resource file as is, note that “default” is set to parameters newly added for Rev. 6.0.

**<padstack.rsc parameter added>**

Parameter	Detailed explanation	Default
gridTable	Defines combination of grid information (grid name, X-direction pitch, Y-direction pitch) that can be selected to specify a grid pitch.	None
ConfirmMode	Specifies whether to display a dialog box to confirm saving. ON : Displays the dialog box. OFF : Does not display the dialog box.	OFF
subCanvas	Maximum number of sub-canvases to display. Specify an integer between 1 and 5.	3

21 parameters are added and two parameters are deleted.

Although you can use this Rev. 5.0 resource file as is, note that “default” is set to parameters newly added for Rev. 6.0.

**<pad.rsc parameter added>**

Parameter	Detailed explanation	Default
gridTable	Defines combination of grid information (grid name, X-direction pitch, Y-direction pitch) that can be selected to specify a grid pitch.	None
penWidthTable	Defines values that can be selected to specify the pen width for line, surface or character.	None
fontName_Motif	Specifies a font name to display cursor coordinates and ruler on the UNIX-version.	“variable”
fontName_MSwindows	Specifies a font name to display cursor coordinates and ruler on the Windows-version.	“Lucida Console/18/Normal”
trapSize	Specifies a search trap side in pixels. Specify 1 or larger integer.	10
ConfirmMode	Specifies whether to display a dialog box to confirm saving. ON : Displays the dialog box. OFF : Does not display the dialog box.	OFF
offsetLineBasePos	Base position used when generating a figure from a line using the offset figure input command. Edge : Outline Center : Center locus	Edge
offsetDeleteBaseFigure	Specifies whether to delete reference figures using the offset figure input command. ON : Deletes. OFF : Does not delete.	OFF
subCanvas	Maximum number of sub-canvases to display. Specify an integer between 1 and 5.	3
viewCoord	Specifies whether to display cursor coordinates on the canvas. ON : Displays. OFF : Does not display.	ON
coordPosition	Display position for cursor coordinates on the canvas. Cursor : Tracks to the cursor. Fix : Fixed on lower right of the canvas.	Cursor
zoomRatio	Zoom ratio. Specify an integer between 5 and 100.	25

panRatioX	Panning ratio in the X-axis direction. Specify an integer between 5 and 100.	50
panRatioY	Panning ratio in the Y-axis direction. Specify an integer between 5 and 100.	50
requestDetail	Specifies the detail mode for the Query Data command. true : Detail mode false : Simple mode	true
ruler	Specifies whether to perform the minimum distance (ruler) display using the Change Shape Attributes command or Query Data command. ON : Displays. OFF : Does not display.	OFF
rulerHeight	Graduated ruler height. Specify a real number (the unit set to unitType is used).	0.1
rulerPitch	Ruler pitch. Specify a real number (the unit set to unitType is used).	0.1
rulerDataSearch	Specifies whether to search data when specifying coordinates with the ruler command. ON : Searches data. OFF : Does not search data.	OFF
rulerXYDistance	Specifies whether to display distances in X- and Y- axis directions when displaying the ruler. ON : Displays. OFF : Does not display.	OFF
tangentArcMode	Automatic tangent arc mode on line, surface (window) and area input. ON : Sets automatic tangent arcs. OFF : Does not set automatic tangent arcs.	OFF

**<pad.rsc parameter deleted>**

Parameter	Detailed explanation
fontName	Deleted because fontName_Motif and fontName_MSwindows are newly set. However, if fontName_Motif is not specified on the UNIX version or fontName_MSwindows is not specified on the Windows version, the value set to this keyword is valid.
searchTrap	Deleted because the way to specify the length of a search trap side is unified with board.rsc. Use trapSize instead.

● **\$ZCSROOT/info/cdbabst.rsc**

**Type (1)**

One parameter is added.

Although you can use this Rev. 5.0 resource file as is, note that “default” is set to parameters newly added for Rev. 6.0.

**<cdbabst.rsc parameter added>**

Parameter	Detailed explanation	Default
ReplaceLcdb	Specifies whether to delete component information defined in the existing LCDB before extraction. true : Deletes. false : Does not delete.	false

● **\$ZCSROOT/info/databook.rsc**

This is a Rev. 6.0 resource file for the newly added Template Definition Tool for the library viewer. This file defines default and parameters for the tool.

● **\$ZCSROOT/info/jpn(eng)/dimrules.dbt**

**Type (1)**

11 parameters are added.

Although you can use this Rev. 5.0 resource file as is, note that “default” is set to parameters newly added for Rev. 6.0.

**<dimrules.dbt parameter added>**

Parameter	Detailed explanation	Default
units	Specifies a unit for dimension line from mm, inch, mil or micron.	mm
assist	Specifies whether to display dimension line auxiliary lines. ON : Displays. OFF : Does not display.	ON
precision	Distance accuracy. Displays the set digits below the decimal point. Specify an integer between 0 and 5.	3
vectorFontName	Font for dimension line text.	zafont0.vec
preString	Character string put before dimension line distance.	"" (Null character)
postString	Character string put after dimension line distance.	mm
arrowShape	Dimension line arrow shape. None, Dot, JIS or ANSI.	ANSI

textWidthRatio	Ratio of dimension line character width to rectangle width enclosing the footprint. Specify an integer between 1 and 100.	4
textHeightRatio	Ratio of dimension line character height to rectangle width enclosing the footprint. Specify an integer between 1 and 100.	4
textSpaceRatio	Ratio of dimension line character interval to rectangle width enclosing the footprint. Specify an integer between 0 and 100.	0
pinpitchXY	"origin/nearest/mostdistant" are added to the existing keywords.	None

● **\$ZCSROOT/info/jpn(eng)/search.rsc**

**Type (1)**

Four search keys are added in (category PadStack "PADSTACK").

**(key "Build-up Via?" (path "isBuildupVia")(selectAble "\*" "Yes" "No"))**

**Target attribute: Build-up Via attribute**

**(key "Hole type" (path "holeType"))**

**Target attribute: hole type**

**(key "Hole diameter or height" (path "holeDiameter\_Height"))**

**Target attribute: round hole diameter, oblong hole diameter and square hole height**

**(key "Hole length or width" (path "holeLength\_Width"))**

**Target attribute: oblong hole length and square hole width**

Paths and candidate list used when specifying a search key for "hole shape" in (category PadStack "PADSTACK") are changed as follows.

Version	Description
Rev. 5.0	(key "hole shape" (path "holeType")(selectAble "*" "circule" "square" "oblong"))
Rev. 6.0	(key "hole shape" (path "holeShape")(selectAble "*" "circule" "square" "oblong"))

● **\$ZCSROOT/info/jpn(eng)/databook.dbt**

**Type (1)**

One parameter is added.

Although you can use this Rev. 5.0 resource file as is, note that “default” is set to parameters newly added for Rev. 6.0.

This resource file has been thoroughly revised in line with release of the Template Definition Tool.

**<databook.dbt parameter added>**

Parameter	Detailed explanation	Default
PinNoJustify	Specifies whether to display the pin number and the reference point to display characters. OFF : Does not display LowerLeft : Lower left LowerCenter : Lower center LowerRight : Lower right MiddleLeft : Middle left MiddleCenter : Center MiddleRight : Middle right UpperLeft : Upper left UpperCenter : Upper center UpperRight : Upper right	OFF

● **\$ZCSROOT/info/jpn(eng)/figure.rsc**

**Type (2)**

Some parameters are added or changed. (Changes are not shown here because this resource file is not available to the public.)

You cannot use this type of resource file for Rev. 5.0 or older as is. If you have changed this file, reflect the changes in the backed up resource file (.bk) to the Rev. 6.0 resource file.

● **\$ZCSROOT/info/jpn(eng)/apptypes.cmm**

**Type (2)**

Some parameters are added or changed. (Changes are not shown here because this resource file is not available to the public.)

You cannot use this type of resource file for Rev. 5.0 or older as is. If you have changed this file, reflect the changes in the backed up resource file (.bk) to the Rev. 6.0 resource file.

14 parameters are added, three parameters are changed, and one parameter is deleted.

Although you can use this Rev. 5.0 resource file as is, note that “default” is set to parameters newly added for Rev. 6.0.

**<board.rsc parameter added>**

Parameter	Detailed explanation	Default
hatchTable	The hatching table (you can specify 1 to 99 hatching tables.) <pre>hatchTable 4 {   Number   "hatching name" interval   angle   ... }</pre> Interval : 5 <=number <=1000 Angle : 0 <=number <360”	None
unit	micron is added to the comment (since Rev. 5.010)	mm
markerFlagSize	Flag mark size (pixel)	15
clrLndDrawMode	Clearance/thermal land display mode (for display without width) none : Not filled in. solid : Filled in black. tone : Black tone pattern	none
fwrdrAnnoUpdate PatternWidth	Specifies whether to reflect the wiring width on the Engineering Design Changing Tool. On : Reflects. Off : Does not reflect.	Off
updateTech FootUpdt	Mode for upgrading footprint data on the PC board with the Board Technology Tool. 0: Compares versions (default). 1: Upgrades all. 2: Does not upgrade.	0
updateTech KeepPadstk	Specifies whether to save In-component figures edited with the Board Technology Tool (padstack). On : Saves. Off : Does not save.	Off
updateTech KeepPad	Specifies whether to save In-component figures edited with the Board Technology Tool (pad). On : Saves. Off : Does not save.	Off
updateTech KeepOther	Specifies whether to save In-component figures edited with the Board Technology Tool (general figures such as line and surface). On : Saves. Off : Does not save.	Off

<p>dynEcoIgnore Jumper</p>	<p>Specifies whether to reflect jumper components targeted for back annotation to the design rule database during active design changing. If a jumper is generated onto the PC board without having been written on the schematics, active design changing deletes the jumper when this value is Off.</p> <p>On : Does not reflect jumper components targeted for back annotation to the design rule database (regards jumper components as a component not targeted for back annotation.)</p> <p>Off : Regards jumper components as normal components.</p>	<p>Off</p>
<p>propForRefHeader</p>	<p>Part property for reference header Specifies the part property setting a reference header.</p> <p>Used to set a default reference header for jumper generation during “component generation” and “wiring input.”</p>	<p>None</p>
<p>useENet</p>	<p>Electrical net operation flag</p> <p>On : Performs electrical net operation.</p> <p>Off : Does not perform electrical net operation</p>	<p>Off</p>
<p>photoErrorSurface</p>	<p>Surface shape adjustment flag Specifies a process when the Artwork, PC Board Outline or Manufacturing Panel Design Tool edits a surface and generates a shape surface for which the aperture-type photo machine cannot perform photo output.</p> <p>notAdd : Does not generate a surface not supporting photo output.</p> <p>adjust : Generates a shape adjusted to support photo output.</p> <p>addAsItIs : Generates a shape surface not supporting photo output.</p>	<p>adjust</p>
<p>requestCmpdiff</p>	<p>Request editing component flag Outputs the following two types of information in addition to <u>edited component information when you select [Request] [PCB Data] [Edited Component]</u> on the Placement/Wiring Tool.</p> <ul style="list-style-type: none"> <li>• Compares objects in the PCB to those in the CDB and outputs objects with different user versions.</li> <li>• Compares footprints referred to by components in the PCB and those related to parts in the CDB and outputs different ones.</li> </ul> <p>0 : Edited component 1 to 3 : Edited component, version comparison and relation comparison 1 to 3 are different in CDB footprints for relation comparison.</p> <p>1 : Compared to default footprints. 2 : Compared to footprints corresponding to footprint specification names. 3 : Compared to all footprints in the package.</p>	<p>0</p>

### <board.rsc parameter changed>

Parameter	Detailed explanation	Difference	
		Rev. 5.0	Rev. 6.0
markerPlusSize	The default is changed.	5	15
markerCircleSize	The default is changed.	5	15
markerCrossSize	The default is changed.	10	15

### <board.rsc parameter deleted>

Parameter	Detailed explanation
MarkerFlageSize	Deleted because this is changed to markerFlagSize. You can set markerFlageSize. If both are set, markerFlagSize (new parameter name) has priority.

## ● \$ZUEROOT/info/propdefs.rsc

**Type (3)**

Some parameters are added or changed. (Changes are not shown here because this resource file is not available to the public.)

You cannot use this type of resource file for Rev. 5.0 or older as is. If you have changed this file, reflect changes in the backed up resource file (.bk) to the Rev. 6.0 resource file.

## ● \$ZUEROOT/info/tpprobe.rsc

This is a newly added Rev. 6.0 resource file that the test point function and the in-circuit tester output program refer to.

## ● \$ZUEROOT/info/jpn(eng)/zfilemgr.rsc

**Type (4)**

This is the secret resource file that tools no longer refer to after upgrading. Nothing is done upon upgrading.

● **\$ZUEROOT/info/jpn(eng)/zfmcustm.rsc**

**Type (4)**

This is the secret resource file that tools no longer refer to after upgrading. Nothing is done upon upgrading.

● **\$ZLOCALROOT/zsys/info/zui.rsc**

**Type (2)**

Some parameters are added or changed. (Changes are not shown because this resource file is not available to the public.)

You cannot use this type of resource file for Rev. 5.0 or older as is. If you have changed this file, reflect the changes in the backed up resource file (.bk) to the Rev. 6.0 resource file.

● **\$ZLOCALROOT/zsys/info/jpn(eng)/zfilemgr.rsc**

This is a newly added Rev. 6.0 resource file.

The user cannot edit this file.

● **\$ZLOCALROOT/zsys/info/jpn(eng)/zfmcustm.rsc**

This is the resource file used to customize the Design File Manager newly added for Rev. 6.0.

Many more commands become available for Rev. 6.0.

If you have customized Rev. 5.0, reflect the changes with one of the following methods.

- With the text editor
- Using the parameter resource load/output function

**With the text editor**

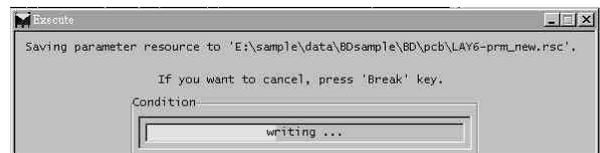
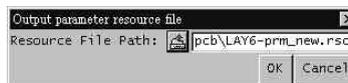
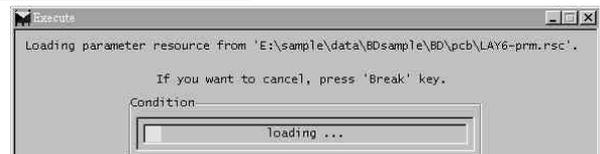
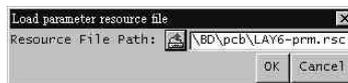
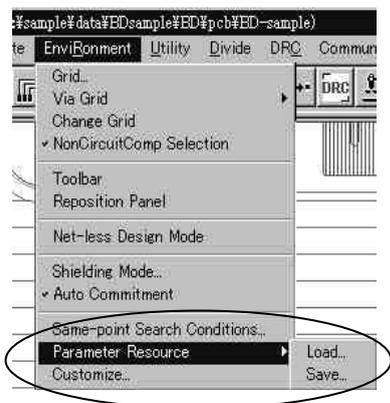
If you can easily identify changed parts and the customized quantity is relatively small, you can reflect them using a text editor such as “vi” or “Wordpad.”

**Using the parameter resource load/output function**

If many parts have been changed, it may be easier to use the parameter resource load/output function available with the Placement/Wiring and Artwork Tools to reflect changes.

**[Operation]**

- (1) Specify a PCB file and start the Placement/Wiring Tool or Artwork Tool. (If you have customized a command related to layer structure such as “visible layer” or “layer attribute,” open the PC board with the same layer structure.)
- (2) Select **[Environment]** **[Parameter Resource]** **[Load...]** on the menu bar.
- (3) Specify the parameter resource file customized on Rev. 5.0 in the Load Parameter Resource File dialog box.
- (4) Clicking **[OK]** loads the parameter resource.
- (5) Then, select **[Environment]** **[Parameter Resource]** **[Output]** on the menu bar.
- (6) Except for customized items, default is stored in parameter resource.



## ● Plotter-related file

The plotter-related file is changed as follows:

- Back up
- \$ZLOCALROOT/zsys/etc/plotEnv.ple parameter added

### Reference

For upgrading the plotting environment, see “1-8 the Plotting Environment Setup Tool Plotting environment upgrade.”

## **Back up**

After upgrading from Rev. 5.0 to Rev. 6.0, reset the plotting environment. Each plotter-related file in the old environment is backed up (copied) upon upgrading.

Back up \$ZLOCALROOT/zsys/bin to \$ZLOCALROOT/zsys/plotback/bin	Post program (postX.sh[bat])
Back up \$ZLOCALROOT/zsys/etc to \$ZLOCALROOT/zsys/plotback/etc	Environment setup file (plotEnv.ple)
	Model file (*.plm)
	Pen table file (*.plp)
	Palette table (*.plt)
	Color table (plotColor.plc)

## **\$ZLOCALROOT/zsys/etc/plotEnv.ple parameter added**

Seven parameters are added.

### **<plotEnv.ple parameter added>**

Parameter	Detailed explanation	Default
GDIMinPen	Plots lines narrower than the specified width without width upon gdidrv.exe execution.	0
GDIAutoDiv	Specifies whether to divide auto-layout data when outputting it to files upon gdidrv.exe execution.	off
GDIR180	Rotates drawing 180° upon gdidrv.exe execution.	off
GDIArc	Specifies arc splitting accuracy upon gdidrv.exe execution. (Currently not used.)	ok
MinPen	Plots lines narrower than the specified width without width.	0
Version	Specifies whether to output files.	old
AutolayDiv	Specifies whether to divide auto-layout data when outputting it to files.	off

# 1-5 Environmental Variable CR5\_PROJECT\_ROOT

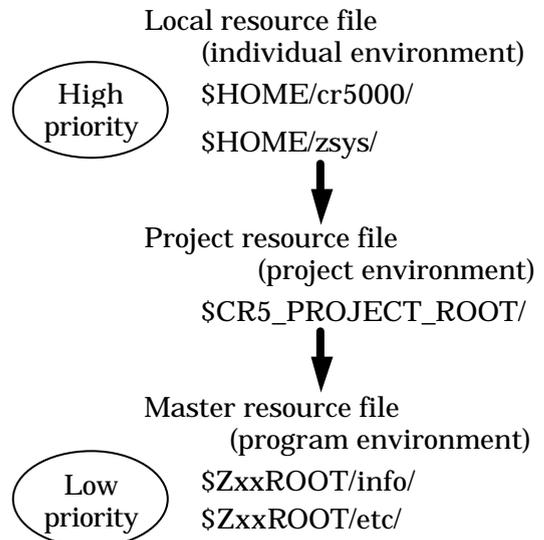
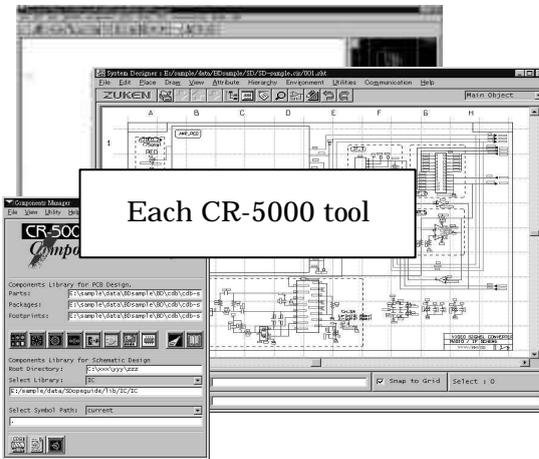


## [Function]

With Rev. 5.0, the master and local resource files can be defined for editing. When two of them are defined, the local resource file has reference priority.

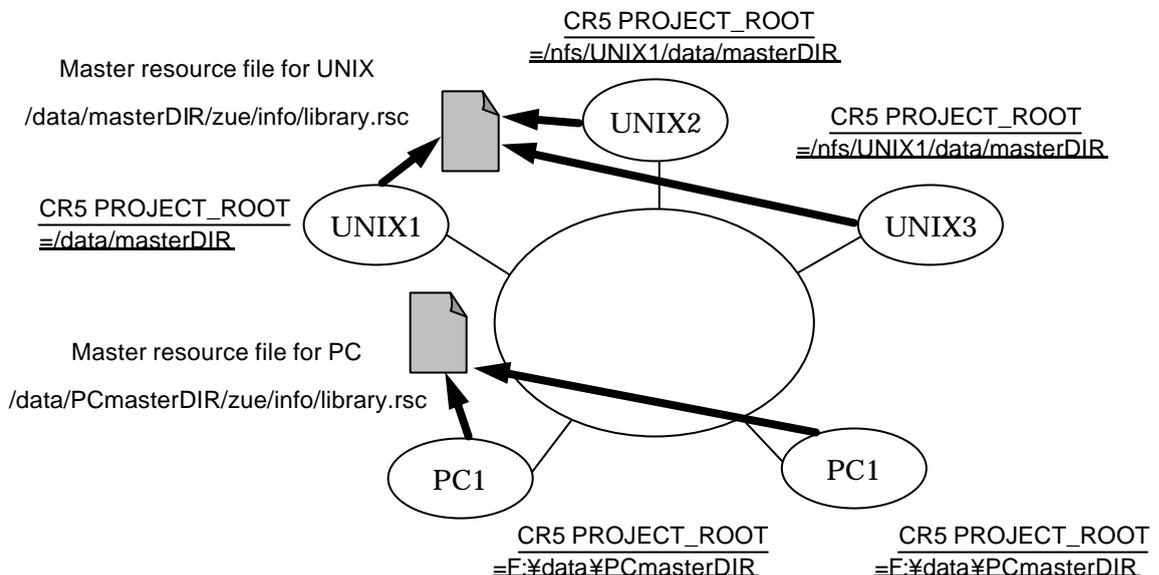
Environmental Variable CR5\_PROJECT\_ROOT is added to Rev. 6.0. The resource file in the directory defined by this environmental variable is called the “project resource file.” This file has reference priority over the master resource file.

This enables efficient management of resource files for server/client operation with multiple clients.



Example: UNIX and PC machines share the PC board library resource file for reference.

(\* Each PC host connects “UNIX1:/” to the F drive.)



## <Directories in the project environment>

Reference tool	Directory containing the project resource file	Directory containing the corresponding master resource file
Common to all tools	\$SCR5_PROJECT_ROOT/zsys/info/	\$ZSYSROOT/info/ \$ZLOCALROOT/zsys/info/
	\$SCR5_PROJECT_ROOT/zue/info/	\$ZUEROOT/info/
System Designer	\$SCR5_PROJECT_ROOT/zds/info/ \$SCR5_PROJECT_ROOT/zds/etc/	\$ZDSROOT/info/ \$ZDSROOT/etc/
Components Manager	\$SCR5_PROJECT_ROOT/zcs/info/	\$ZCSROOT/info/
Board Designer	\$SCR5_PROJECT_ROOT/zpls/info/ \$SCR5_PROJECT_ROOT/zpls/etc/	\$ZPLSROOT/info/ \$ZPLSROOT/etc/
Board Producer	\$SCR5_PROJECT_ROOT/zpms/info/ \$SCR5_PROJECT_ROOT/zpls/etc/	\$ZPMSROOT/info/ \$ZPMSROOT/etc/

### [Notes and Restrictions]

- If there are machines with different Kanji codes in an environment (e.g. HP and SUN versions), you should define the keywords to identify the Kanji code in the resource file. Before moving the existing resource file to the directory containing the project resource file, check that the identification keyword for the Kanji code exists.

If any identification keyword is not defined, the standard Kanji code for the platform where the program is executed (HP, PC = sjis, SUN = euc) is used for loading. This may cause unexpected results.

#Japanese_coding:      sjis or euc
------------------------------------

- Some types of resource files cannot be shared on PC and UNIX versions. If you are using PCs and UNIXs in a mixed environment, you need different directories to store each project resource file.

```
$SCR5_PROJECT_ROOT/zsys/info/jpn(eng)/zfmcustm.rsc
$SCR5_PROJECT_ROOT/zds/info/lancolor.rsc
$SCR5_PROJECT_ROOT/zds/etc/jpn(eng)/battool.rsc
$SCR5_PROJECT_ROOT/zue/library.rsc
```

- Only the resource file with the highest priority is loaded according to the reference priority of their saving directories. With a previous version, some of the programs that load board.rsc and library.rsc opened all files in the reversed order and loaded definitions. The specifications are changed in line with the addition of the project resource file so that all programs load only priority files.

### Reference

For details on operation, see “CR-5000 User’s Guide/7.1.2 Project resource file.”



# 1-7 Design File Manager



The following functions are added or improved for the Design File Manager (old name: Board File Manager).

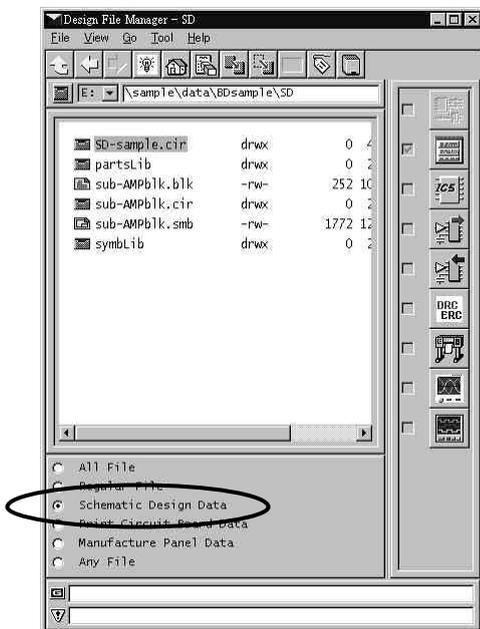
- Integration with the SD File Manager
- Improved tool box
- Schema evolution (Database Conversion Program)
- Batch data compaction function
- Drive selector support (Windows version only)
- Action execution (Windows version only)

## ● Integration with the SD File Manager

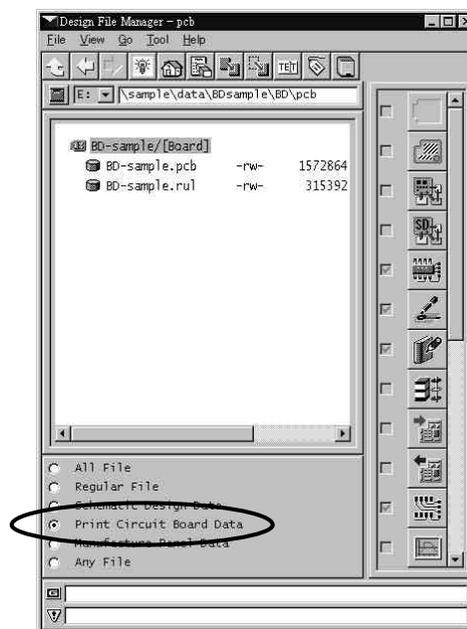
### [Function]

Integration with the SD File Manager functions enables the starting of an SD tool and processing of data from this tool and CR-5000 file manager unification.

Accordingly, the Board File Manager has been renamed the Design File Manager.



<[Schematic Design Data]  
is selected as filter>

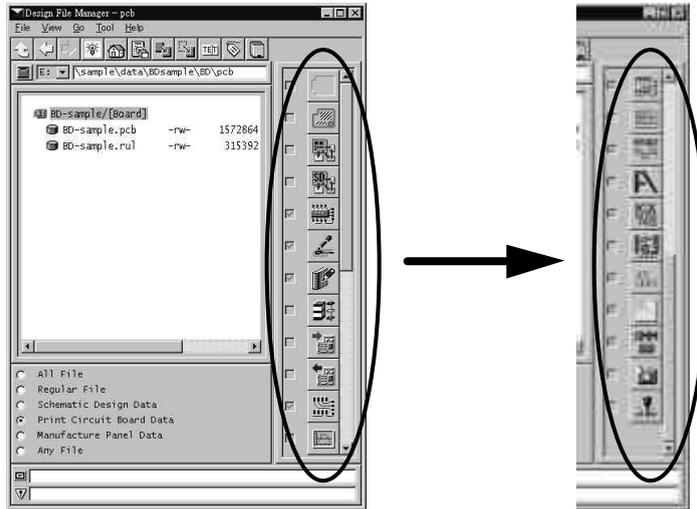


<[Print Circuit Board Data]  
is selected as filter>

## ● Improved tool box

### [Function]

You can customize your resource file by specifying the minimum number of tool buttons displayed and the tool names not to be displayed in the tool box (zfmcustm.rsc).

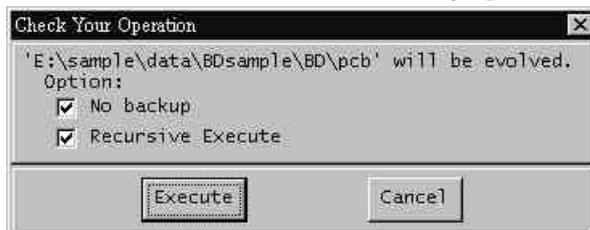


## ● Schema evolution (Database Conversion Program)

### [Function]

You can specify options added for Rev. 6.0 with the Design File Manager when schema evolution (Database Conversion Program) is executed.

- Does not create a back up file
- Recursive execution (for directory specification only)



### [Operation]

- (1) Select a database file or directory (folder).
- (2) Select **Tool** **Action** **Schema Evolution** from the menu bar.

### Reference

For schema evolution (database conversion) program, see "1-1 Converting Databases from Rev. 5.0 to Rev. 6.0."

## ● Batch data compaction function

### [Function]

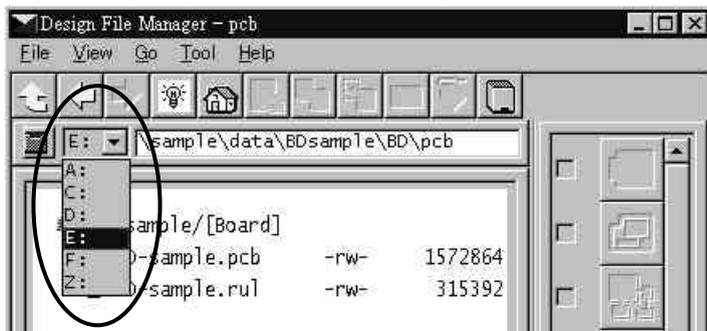
Rev. 6.0 supports a function to compact the PC board and panel data per directory and a display function enabling the user to easily see if compacting is necessary.

BD-sample/[Board]  
BD-sample.pcb  
BD-sample.rul

## ● Drive selector support (Windows-version only)

### [Function]

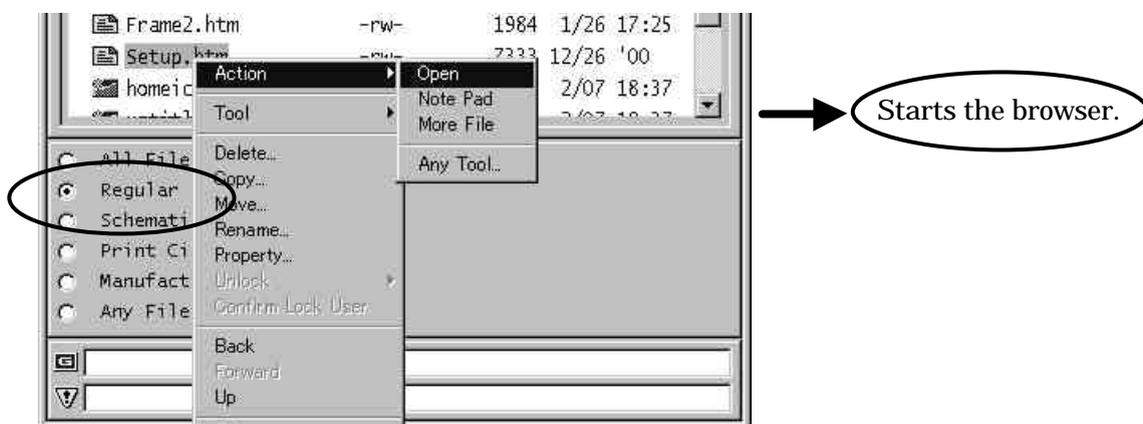
You can specify a drive from the option list.



## ● Action execution (Windows-version only)

### [Function]

With Rev. 6.0, you can open a file using the corresponding Windows tool when CR-5000 and all other data files are displayed with "Regular File" etc. selected as filter.



# 1-8 Plotting Environment Setup Tool



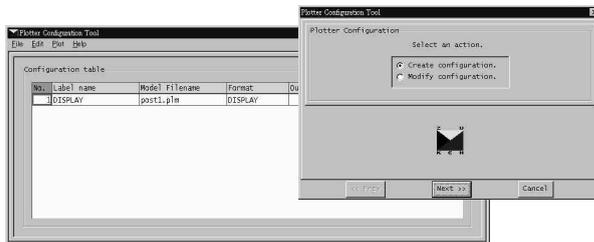
The following functions are added or improved for the Plotting Environment Setup Tool.

- Common to UNIX and Windows versions
- Detailed setting for model files
- Dimension line parameter
- Test and sample plotting support (Windows version)
- Plotting environment upgrade

## ● Common to UNIX and Windows versions

### [Function]

The Plotting Environment Setup Tool is made common to the UNIX and Windows versions. You can register and change the plotting environment using the Wizard.



### [Operation]

- (1) Start the Plotting Environment Setup Tool.

#### [UNIX version]

Execute the following command in the Super User mode.

```
#$ZLOCALROOT/zsys/bin/pltcnf.sh
```

#### [Windows version]

Select **Program** **CR-5000 PCB Layout System** **Plotter Setting** from the start menu. (You do not need the administrator privilege.)

- (2) Set up by following the directions for the Wizard.

### Reference

If “the Plotter Configuration Upgrade dialog box” appears on Plotting Environment Setup Tool activation, see “Plotting environment upgrade” in this chapter.

## ● Detailed setting for model files

### [Function]

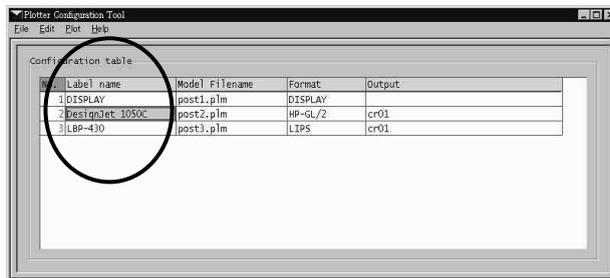
You can set each model file in detail from the menu.

The following items are settable.

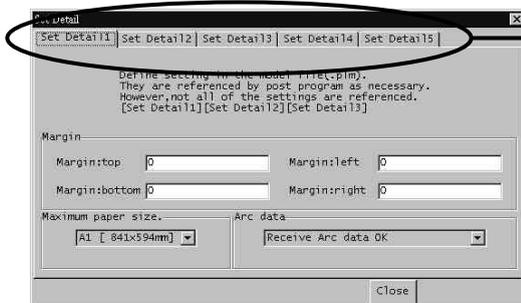
Tab	Setting		
Set Detail 1	Margin	Maximum paper size	Arc data permission
Set Detail 2	Plotting origin position	Auto-cut function permission	Overwriting permission
	Arc-in-polygon permission	Rectangle data permission	Maximum number of polygon vertexes
	180° rotation settings for output	Auto-layout function permission	
Set Detail 3	Font plotting mode	Maximum number of pens	Maximum number of palettes
Set Detail 4	Color table	Pen table	Palette table
Set Detail 5	Minimum pen width	Auto-layout data split setting	

### [Operation]

- (1) Select a model file to edit on the Plotting Environment Setup Tool.



- (2) Click **Edit** **Change** from the menu bar.
- (3) After the plotting environment setup Wizard starts, click **Next** on the Input Label Name screen.
- (4) Click **Set Details** at the bottom of the Specify Model File screen to start the Set Detail dialog box.



You can set Set Detail 1 to 5 by switching tabs.

- (5) When detail setting is complete, end the operation by following the directions for the Wizard.

## ● Dimension line parameter

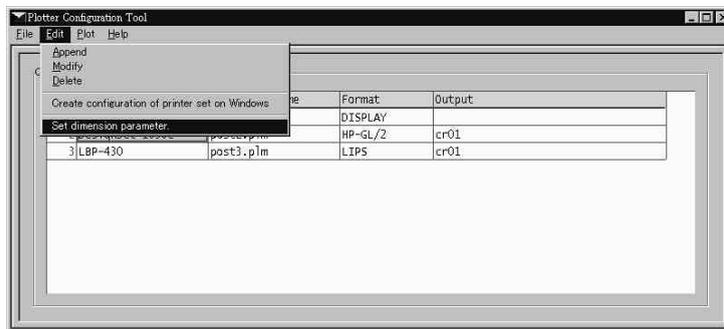
### [Function]

When scaling and plotting data containing a dimension line, you can specify whether to scale the dimension line as well. Select one of the following processes for dimension lines.

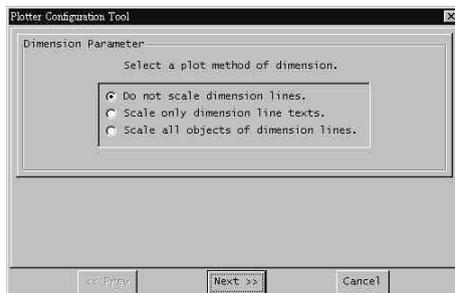
- Does not scale the dimension line
- Scales only the dimension line text
- Scales the whole dimension line

### [Operation]

- (1) Click **Edit** **Set dimension parameter** from the Plotting Environment Setup Tool menu bar.



- (2) Specify a dimension line plotting method in the Dimension Parameter Wizard.



- (3) When detail setting is complete, end the operation by following the directions for the Wizard.

### [Notes and Restrictions]

- For dimension line plotting setting, Environmental Variable

“ZPLOT\_DIM\_SCALE” has priority if this is set.

ZPLOT\_DIM\_SCALE =0 Does not scale the dimension line.

ZPLOT\_DIM\_SCALE =1 Scales the dimension line text.

ZPLOT\_DIM\_SCALE =2 Scales the whole dimension line.

- On “X-Window” output and “LIPS,” “HP- GL” file output, all data is scaled regardless of settings for dimension line parameters and Environmental Variable “ZPLOT\_DIM\_SCALE.”

## ● Test and sample plotting support (Windows version)

### [Function]

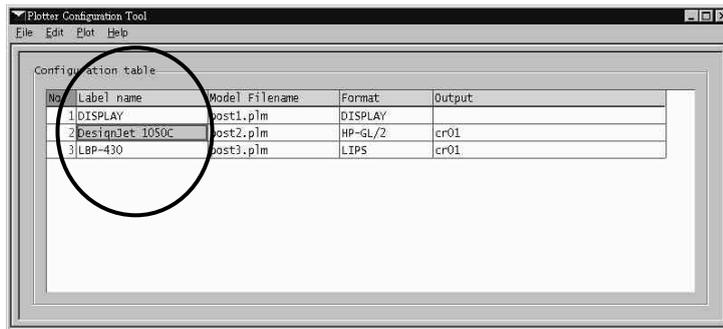
The **Windows** version Rev. 5.0 does not have a test plotting function while the **UNIX** version does. The sample plotting function is started in batch on the **Windows** version.

With Rev. 6.0, you can perform test and sample plotting using the Plotting Environment Setup Tool. In test plotting, a rectangle is plotted on an appropriate size of paper by referring to the model file. This enables immediate testing of the set environment.

Pen and palette samples can be plotted on a specified paper-size only with the electrostatic plotter.

### [Operation]

- (1) Select a model file for test or sample plotting on the Plotting Environment Setup Tool.



- (2) Click **Plot**, **Test Plot** or **Sample Drawing** from the menu bar.

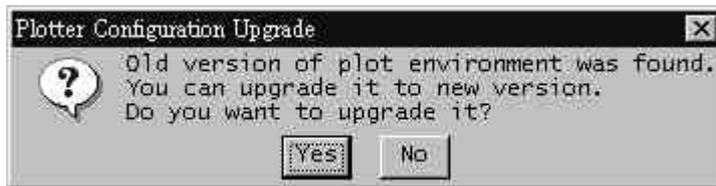
## ● Plotting environment upgrade

### [Function]

After upgrading Rev. 5.0 to Rev. 6.0, the plotting environment should be reset. The upgrade function for the plotting environment refers to the old environment and automatically builds a new environment with the same setting.

### [Operation] (execution with the dialog box)

- (1) If you have set a plotter environment, the confirmation dialog box for upgrading appears when the Plotting Environment Setup Tool is started for the first time after upgrading to Rev. 6.0.



- (2) Clicking  automatically upgrades the plotting environment.
- (3) If a printer model file exists on the UNIX version, a dialog box confirming overwriting appears subsequently.
- (4) When upgrading is complete, the exit dialog box appears ending the tool. To add, change or delete settings, restart the tool.

Upgrading creates or updates files in the following locations.

\$ZLOCALROOT/zsys/bin	Post program (postX.sh, postX.bat)
\$ZLOCALROOT/zsys/etc	Environment setup file (plotEnv.ple)
	Model file (postX.plm)
	Pen table file (postX.plp)*
	Palette table (postX.plt)*
	Color table (postX.plc)

Files indicated by an asterisk (\*) may not be created depending on the format.

### [Notes and Restrictions]

- The [\$ZLOCALROOT/zsys/plotback/up.end] file is created when upgrading is performed. This file is also created when operation is canceled. If this file exists, the upgrade dialog box is not displayed. To upgrade the plotting environment after cancellation, delete the [up.end] file before starting the Plotting Environment Setup Tool.
- If you have manually set the post program in the old environment, modify the post program after upgrading.

## [Operation] (batch execution)

To start the Plotting Environment Upgrade command (zplotevolve), enter the following.

```
zplotevolve.exe Required parameter [Optional parameter]
```

\* On the UNIX version, the Super User should start this command.

### 1. Required parameter

**-p: dir** Directory name containing the environment setup file, plotEnv.ple

Directory name containing the setup file [PlotEnv.ple] for the old environment.

If Rev. 5.0 is upgraded, the default is \$ZLOCALROOT/zsys/plotback/etc.

### 2. Optional parameters

**-p: overwrite** the overwrite mode for the printer model file

Valid only on the UNIX version.

Specifies to overwrite the printer model file.

Specify on or off.

\* If this is omitted, the default is off.

**-h**

Displays usage.

**-v**

Outputs version information.

## [Notes and Restrictions]

- The [up.end] file is not created when upgrading is performed with the batch program.
- If you have manually set the post program in the old environment, modify the post program after upgrading.

# 1-9 Plotting PC board



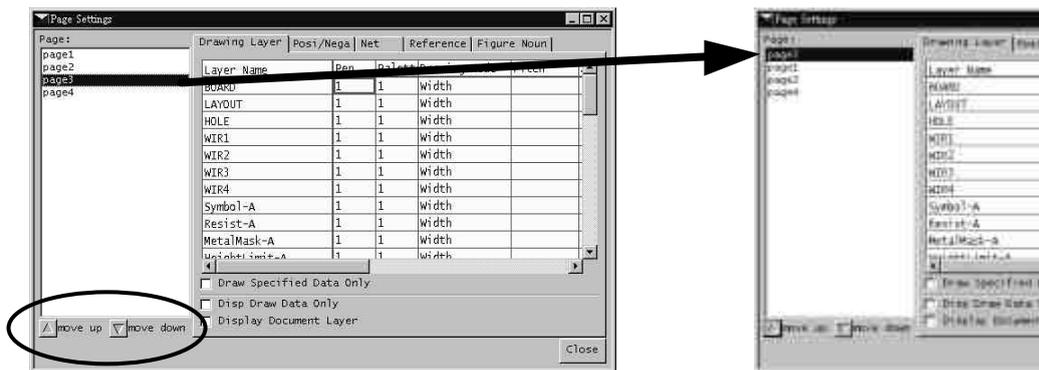
The following functions are added or improved for the PC Board Plotting Tool.

- Function added to specify the output order
- Function added to filter objects to output
- File output function added for the post program
- Improved character mirroring
- Added plotting mode “Paint”

## ● Function added to specify the output order

### [Function]

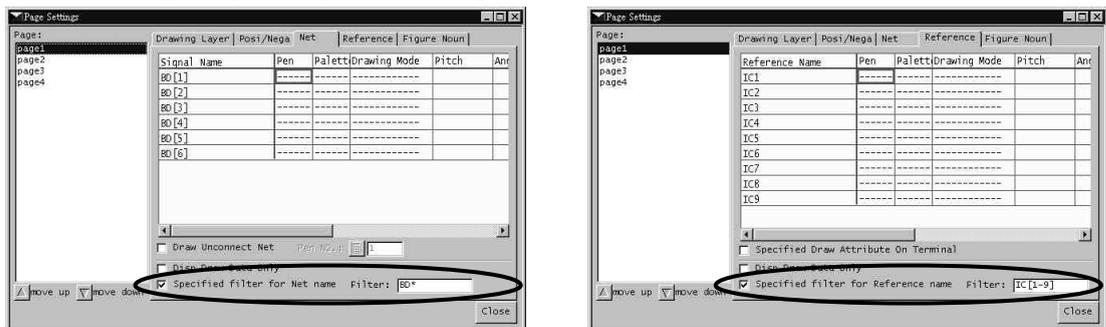
When you set multiple plotting pages, plotting is performed in the order that they are set. With Rev. 6.0, you can freely change the plotting page order.



## ● Function added to filter objects to output

### [Function]

With Rev. 6.0, you can filter and narrow down net and reference names for display when setting the plotting attributes per net or reference.

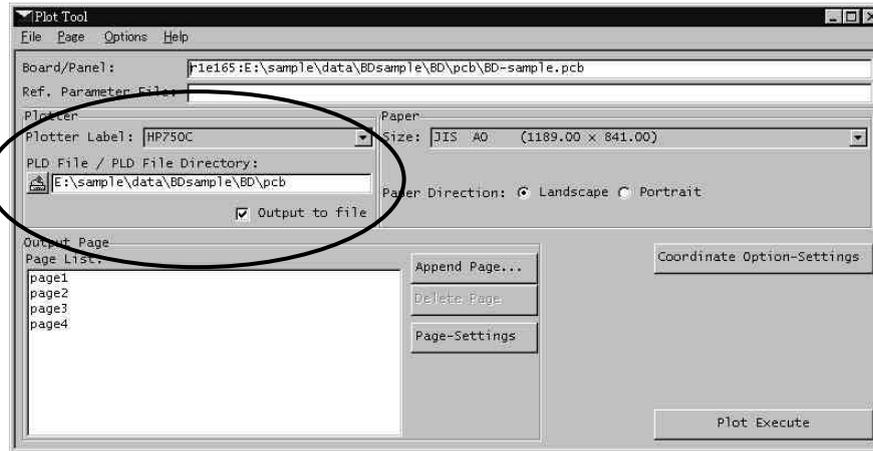


## ● File output function added for the post program

### [Function]

Rev. 5.0 can output data in only four formats: “CR-5000,” “CR-3000,” “HP-GL” and “LIPS.”

With Rev. 6.0, you can output data to other post programs. This enables data output that has been directly output to the plotter or printer as a plotting intermediate file.

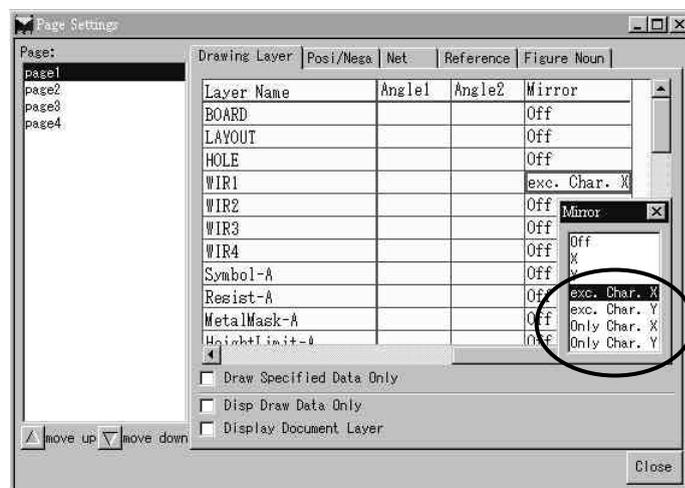


## ● Improved character mirroring

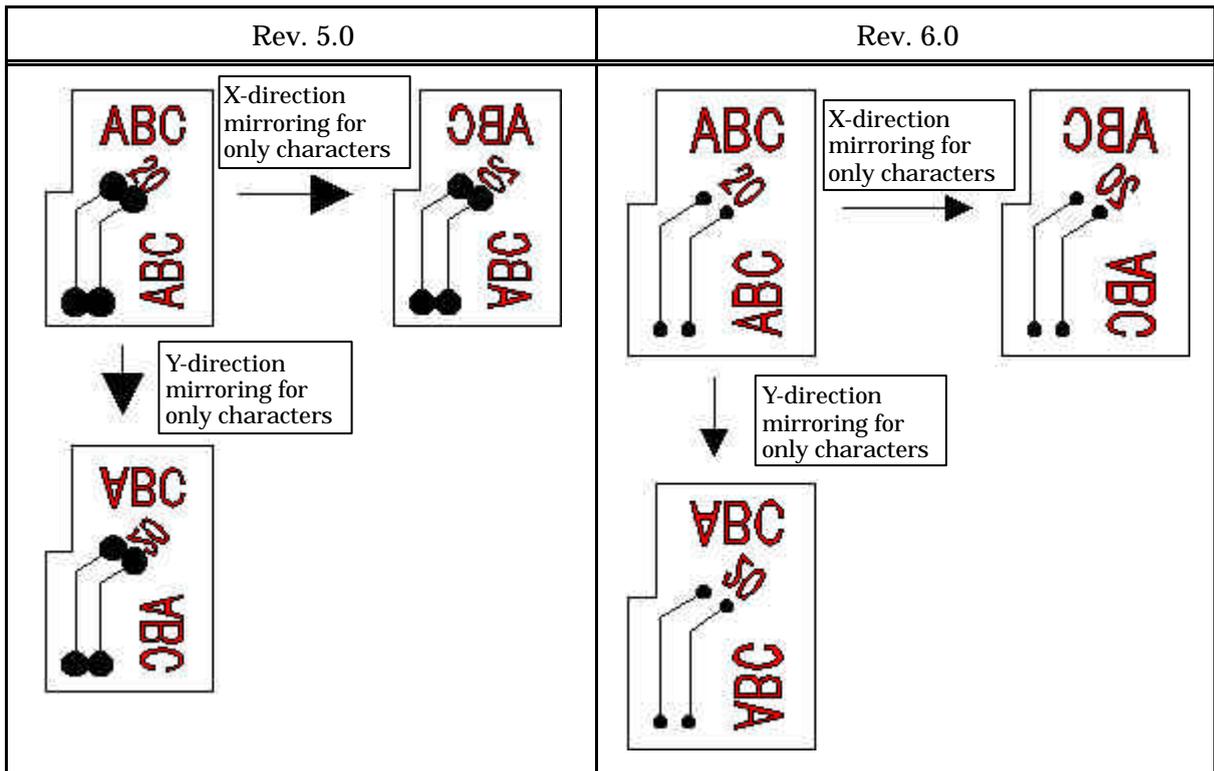
### [Function]

With Rev. 5.0, character mirroring is performed in the X- or Y-axis direction on the display.

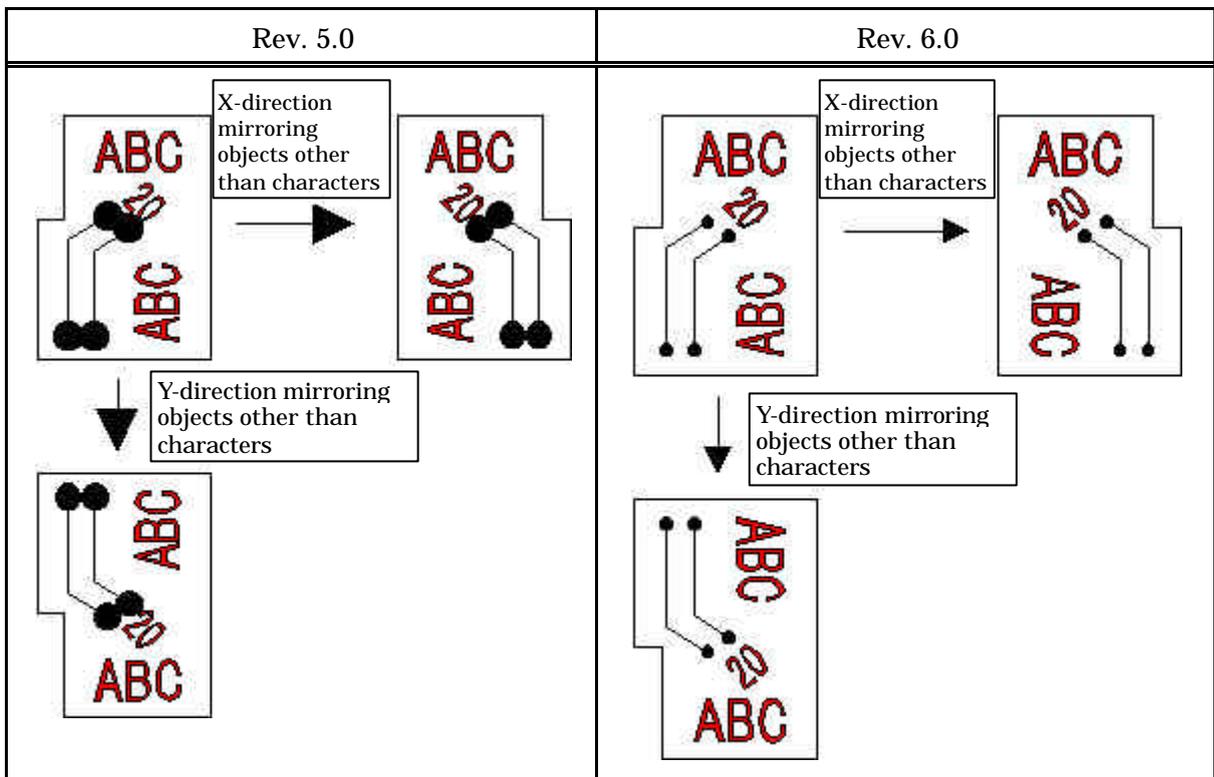
When the mirror mode is “character exclusion” or “character only” on Rev. 6.0., X-mirroring is performed based on the line horizontal to characters and Y-mirroring is performed based on the line vertical to characters.



**<Mirroring only characters>**



**<Mirroring objects other than characters>**



**[Notes and Restrictions]**

- Processing in the “X-direction” and “Y-direction” mirror modes has not been changed.

## ● Added plotting mode “Paint”

### [Function]

Rev. 5.0 has five plotting modes: “without width,” “with width,” “tone,” “hatching 1” and “hatching 2.”

Rev. 6.0 features the “painting” mode in addition to these.

In the “painting” mode, the electrostatic plotter plots outlines with width on objects plotted in the tone mode. This enables tone plotting with outlines.

### [Notes and Restrictions]

- The pen plotter does not support tones. If the “tone” or “paint” mode is employed for the pen plotter, this results in plotting with width.

# 1-10 Enhanced Print Command



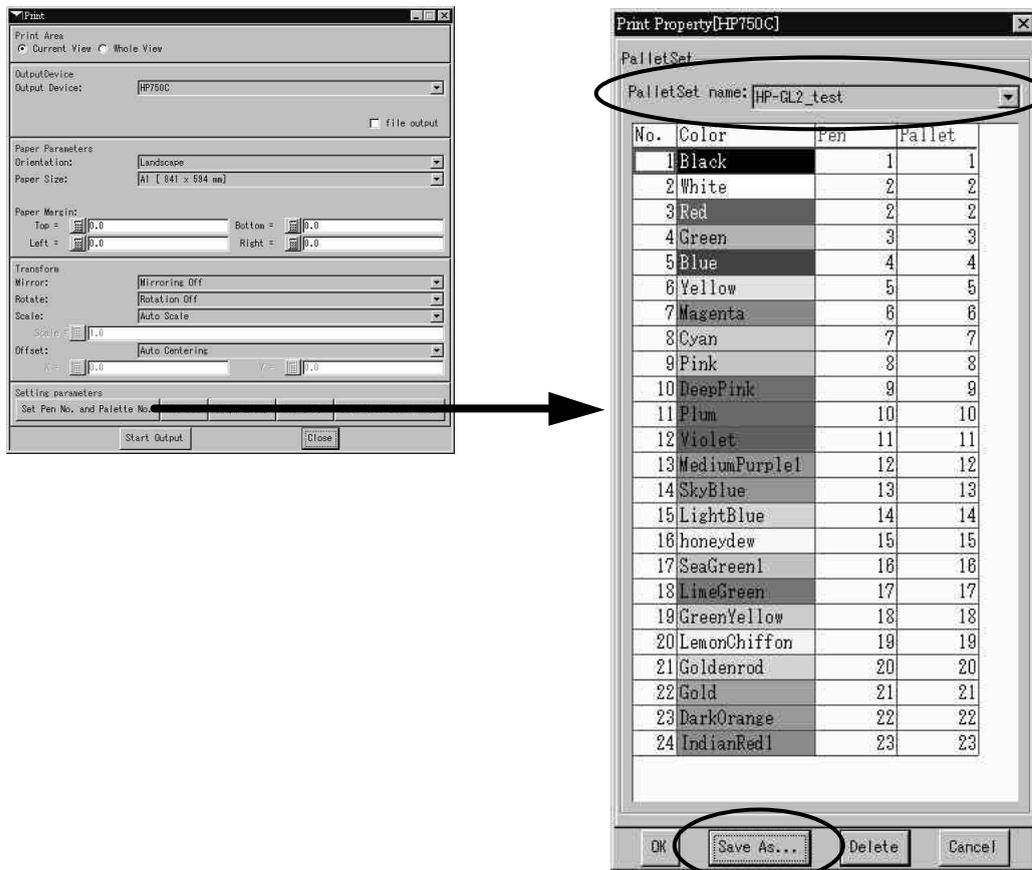
The following functions are added or improved for the Print command.

- Saving specified pen and palette numbers to a file
- File output function added for the post program
- Display mode for clearance and thermal land support
- Improved screen display

## ● Saving specified pen and palette numbers to a file

### [Function]

With Rev. 6.0, you can save the setting for the pen and palette tables to a file and load the file. You can also specify different files to load for each output device. This saves you the time and work in resetting the pen and palette numbers every time.

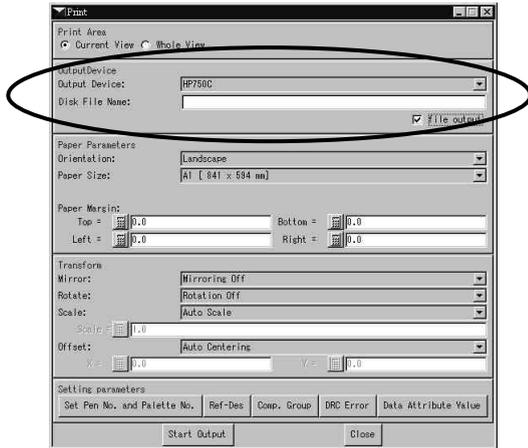


## ● File output function added for the post program

### [Function]

Rev. 5.0 can output data in only four formats: “CR-5000,” “CR-3000,” “HP-GL” and “LIPS.”

With Rev. 6.0, you can output data to other post programs. This enables data output that has been directly output to the plotter or printer as the plotting intermediate file.



## ● Display mode for clearance and thermal land support

### [Function]

With Rev. 6.0, you can change the display mode for thermal and clearance land by changing board.rsc. In other words, you can specify thermal or clearance land display when displaying them with width. Correspondence with board.rsc setting and output with the Print command is shown below.

board.rsc(clrLndDrawMode) setting	Output with the Print command
none (not filled)	With width
solid (filled in black)	Outlined in black
tone (black tone pattern)	With width

### Reference

For the display mode for thermal and clearance land, see “4-15 Improved Display Function ? Negative figure display mode for display with width is made resource.”

## ● Improved screen display

### [Function]

Screen display is improved as follows for Rev. 6.0. Accordingly, the Print command now can perform printing corresponding to each screen display. You do not need special settings for printing with the Print command. Image displayed on the screen is plotted as is.

- Component reference point display
- Hatching and tone display per net
- Panel data display
- Panel design reference display

### Reference

For the component reference point display, hatching and tone display per net and panel data display function, see “4-15 Improved Display Function.”

For the panel design reference display function, see “6-1 Enhanced Manufacturing Panel Design Tool Function ? Reference display.”

### [Notes and Restrictions]

- On displaying hatching and tone per net, nets with tone are plotted in the “with width” mode.

# 1-11 Document Designer



The following functions are added for the Document Designer.

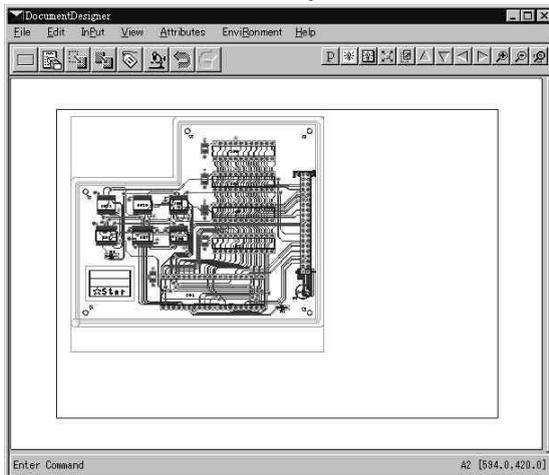
- Load HP-GL or HP-GL2 format data
- Increase in the attributes that can be changed
- Editing table frame lines
- Grid support
- Undo and redo support

## ● Load HP-GL or HP-GL2 format data

### [Function]

Rev. 5.0 can load only three types of files: “text file,” “CSV file” and “CR-5000 plot intermediate file.”

Rev. 6.0 can additionally load “HP- GL file” and “HP- GL2 file.”



### [Operation]

- (1) Input a frame to load HP- GL or HP- GL2 data by selecting **Input** **Input Data** **Frame** from the menu bar.
- (2) Move the mouse cursor onto the frame where data is to be loaded, and then display the Assist Menu.
- (3) Select **Read data?** **Other Data Format** on the Assist Menu.
- (4) Select an HP- GL or HP- GL2 data file from the File Selector dialog box.

### [Notes and Restrictions]

- You cannot load HP- GL or HP- GL2 data to table and group frames.
- Dashed lines are loaded as a solid line.

## ● Increase in the attributes that can be changed

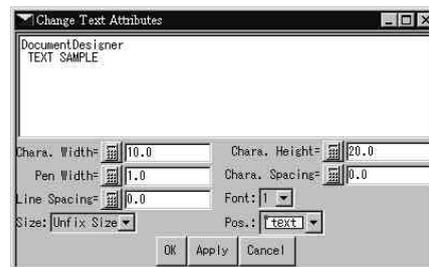
The following attributes for input data can be changed.

- Character attributes
- Table frame attributes
- Plot intermediate data frame attributes

### **Character attributes**

#### **[Function]**

You can fix the size of the character parameters and the text frame, and also change the character position in the frame. If the size of the frame is [Fixed], the character size does not change even if the frame size is changed. If the size is [Not Fixed], the character size is maximized as the frame size changes. The character width, character height, pen width, character interval and line interval parameters represent the actual size if the size is [Fixed], and the parameter ratio if the size is [Not Fixed].



#### **[Operation]**

- (1) Move the cursor onto the text frame.
- (2) Click **Change Attribute** on the Assist Menu.
- (3) Set parameters with the displayed Character Attribute Changing dialog box.
- (4) Click **OK** or **Apply** to reflect the new settings.

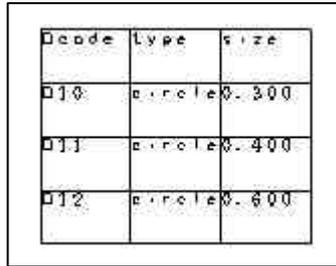
#### **[Notes and Restrictions]**

- If the size is [Fixed], a large character string may run off the edge of the frame.

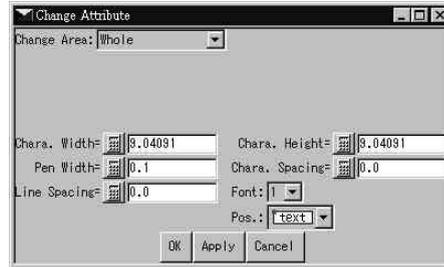
## **Table frame attributes**

### **[Function]**

You can change the character attributes in the table frame where a CSV file is loaded.



Code	Type	Size
010	circle	0.300
011	circle	0.400
012	circle	0.600



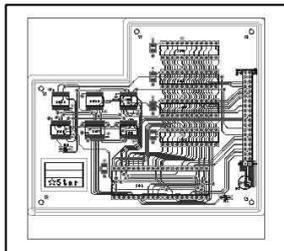
### **[Operation]**

- (1) Move the cursor onto the table frame.
- (2) Click **Change Attribute** on the Assist Menu.
- (3) Set parameters with the displayed Character Attribute Changing dialog box.
- (4) Click **OK** or **Apply** to reflect the new settings.

## **Plot intermediate data frame attributes**

### **[Function]**

You can fix the size of the plot intermediate data frame and also change the character position in the frame. If the size of the frame is [Fixed], the plot intermediate data is displayed in the same size as the original size. In this case, plot size does not change even if the frame size is changed. If the size is [Not Fixed], the plotting size is automatically maximized as the frame size changes.



### **[Operation]**

- (1) Move the cursor onto the data frame where the plot intermediate data has been loaded.
- (2) Click **Change Attribute** on the Assist Menu.
- (3) Set parameters with the displayed Character Attribute Changing dialog box.
- (4) Click **OK** or **Apply** to reflect the new settings.

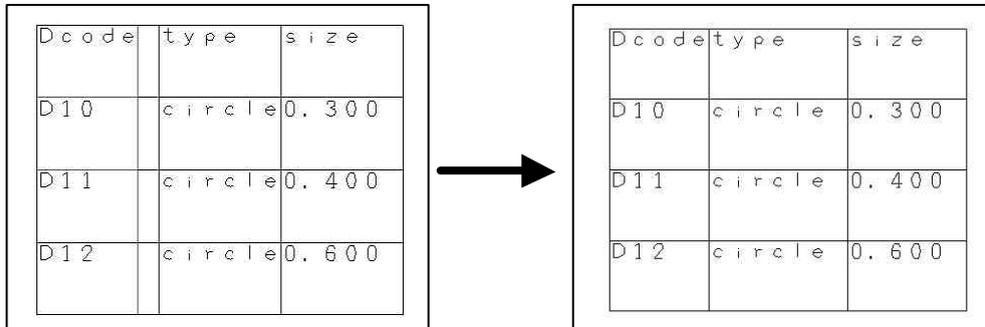
### **[Notes and Restrictions]**

- If the size is [Fixed], a plot may run off the edge of the frame depending on the specified plot intermediate data size.

## ● Editing table frame lines

### [Function]

You can move a table frame line to change the height or width for a line or column. Text in the table moves in line with the changed table.



Dcode	type	size
D10	circle	0.300
D11	circle	0.400
D12	circle	0.600

### [Notes and Restrictions]

- Text in the frame may run off the edge of the frame depending on how much the table frame line is moved.
- A frame line can be moved within adjacent cells.

## ● Grid support

### [Function]

You can set a grid. Grid retraction is performed according to grid display.

### [Operation]

- (1) Select **Environment** **Grid** from the menu bar.
- (2) Set a grid on the displayed Grid Setup dialog box.
- (3) Select **View** **Grid** from the menu bar.
- (4) This switches whether to display and retract the grid.

## ● Undo and redo support

### [Function]

Rev. 6.0 supports undo and redo operations.

### [Notes and Restrictions]

- Rev. 6.0 can undo or redo once.

# 1-12 Expanded Customization Function



The following functions are expanded for customization.

- Macro command editor support
- Opening and closing the user menu
- Improved customized-environment function
- Customized tool bar and menu bar supporting Rev. 6.0

## ● Macro command editor support

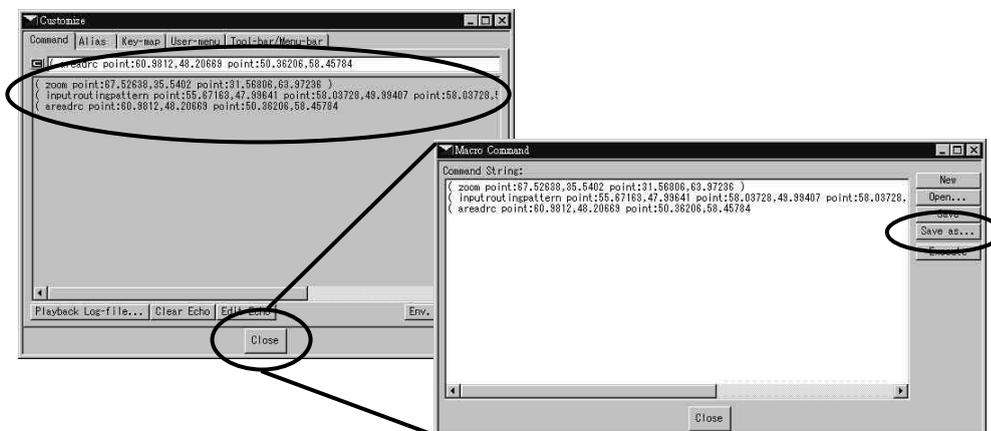
### [Function]

The Editor dialog box is added for user macro command (alias and log file).

The same data as the character string (token) for the operation saved to the log file is output (Echo output) to the Customization dialog box. This facilitates editing, saving, saving a specified macro command in another name and executing macro commands being edited.

### [Operation]

- (1) Click **Edit Echo** in the Customize dialog box to start the Macro Command dialog box.
- (2) The Macro Command dialog box displays Command echo.
- (3) Edit command character strings and click **Save as...**



## ● Opening and closing the user menu

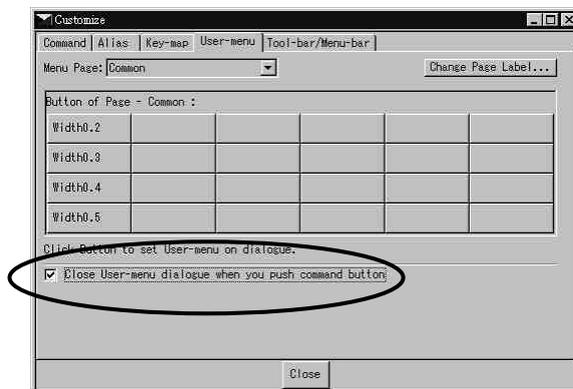
The following functions are added for the user menu.

- Automatic closing
- Start with a shortcut key

### **Automatic closing**

#### **[Function]**

You can set automatic closing of the dialog box when the command button is selected (clicked) in the user menu dialog box.



### **Start with a shortcut key**

#### **[Function]**

The shortcut key “Ctrl+M” functions the same as when you select **Utility** **User** **menu**.

## ● Improved customized-environment function

The following functions are improved for the customized environment.

- CLUI macro-variable support
- “End all active commands” function support
- Escape characters
- Naming aliases
- Command Log “next” token changed

### **CLUI macro-variable support**

#### **[Function]**

The command character string user interface (hereafter, “CLUI”) for Rev. 6.0 supports the following macro variables (they store tool information and are dynamically updated in line with tool status).

This enables use of these macro variables when creating a user menu command during customization using CLUI.

- DB file path being edited            `${dbPath}`
- Current mouse cursor coordinates   `${cursorPointX}`, `${cursorPointY}`
- Real-time search coordinates        `${realSearchPointX}`, `${realSearchPointY}`

### **“End all active commands” function support**

#### **[Function]**

This function forcibly terminates (cancels) active commands (including interrupt commands) and makes all commands for the tool inactive. If commands are not active, nothing is performed. By writing this before the command character string, you can assign a command that cannot be started until the other commands are terminated.

resetCommand

Example)

resetCommand (inputroutingpattern automode: “jump”

## **Escape characters**

### **[Function]**

The instructions for specifying escape characters have been changed in the case when the CLUI token character string type argument contains a character to be escaped from (“\ (backslash)” and “” (double quotation))”).

Version	Specifying escape characters
Rev. 5.0	To escape out of a character in a character string type argument (“\” and “””), add three backslashes “\” before the character.
Rev. 6.0	To escape out of a character in a character string type argument (“\” and “””), add one backslash “\” before the character.

### **[Notes and Restrictions]**

If you have customized the Rev. 5.0 environment, perform the following operation.

Change three backslashes “\” to one in the customization definitions existing for aliases, key maps, the user menu and tool bar.

You do not have to change the log file.

## **Naming aliases**

### **[Function]**

To use customized aliases with Rev. 6.0, you should specify an alias name followed by “@uals”.

For example, if you have defined Alias “userCmd” with the Macro Command Editor and want to use this in a CLUI character string, you should write “userCmd@uals”.

### **[Notes and Restrictions]**

If you have customized the Rev. 5.0 environment, perform the following operation.

If the existing alias, key map, user menu, tool bar or the command character string in the log file uses an alias, add “@uals” after the alias.

If any alias-is not used, you do not have to change it.

## **Command Log “next” token changed**

### **[Function]**

The CLUI [next] token specifications are changed because the real-time search for the wiring and surface input functions of the Placement/Wiring Tool supports command log on Rev. 6.0.

Version	Changed and new specifications for the [next] token
Rev. 5.0	next (no colon, no argument)
Rev. 6.0	next:{\$cursorPointX},{\$cursorPointY},{\$realSearchPointX},{\$realSearchPointY} (colon, four arguments)  {\$cursorPointX} : X-coordinate for the current cursor position {\$cursorPointY} : Y-coordinate for the current cursor position {\$realSearchPointX} : X-coordinate on real-time search {\$realSearchPointY} : Y-coordinate on real-time search  (Values to these arguments can be used as macro variables without modification.)

### **[Notes and Restrictions]**

If you have customized the Rev. 5.0 environment, perform the following operation.

- [next] setting in the key map/alias/menu bar

If the key map and other environments are customized and use [next] token, reset as follows:

```
next:{$cursorPointX},{$cursorPointY},{$realSearchPointX},{$realSearchPointY}
```

However, the customization key map “n” does not have to be processed as long as the [next] token (default for the “n” key) is set because the tool automatically resets as above.

- Rewriting the existing command log file (\*.log)

If the existing command log file contains the [next] token, rewrite the existing command log file as follows:

```
next:0,0,0,0
```

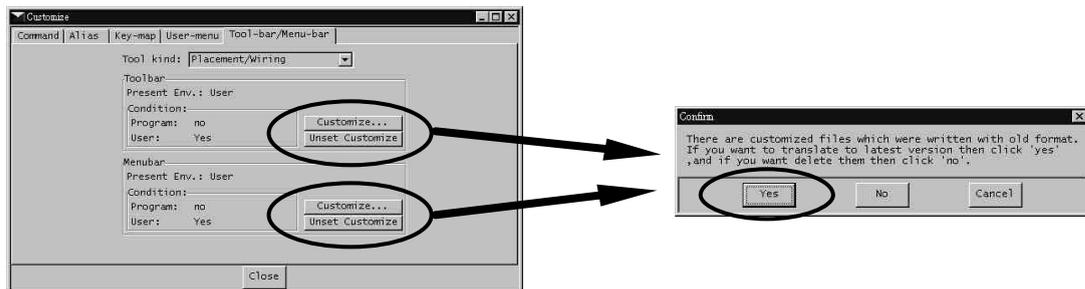
## ● Customized tool bar and menu bar supporting Rev. 6.0

### [Function]

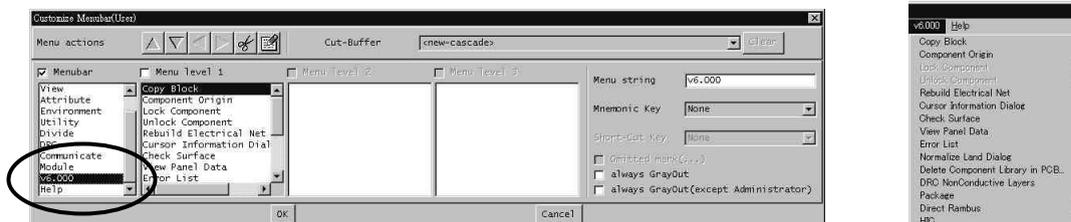
Rev. 6.0 has new commands for interactive design. If you have customized the environment per individual or program by using the “menu bar/tool bar customize” function provided to CR-5000/BD or BP interactive design modules, update the customized definition environment.

### [Operation]

- (1) Start a BD or BP module and then start the Customization dialog box by selecting **Environment** **Customize** from the menu bar.
- (2) Click **Customize...** on the “Tool-bar/Menu-bar” tab under “Menu bar” or “Tool bar.” (If you have not customized the previous version, **Unset Customize** is shaded and unavailable.)
- (3) If a customized file for the previous version exists, the confirmation dialog box asking whether to convert it to the current version format or delete it will appear.
- (4) Click **Yes**.



The next pages list additions to modules on the menu bar. If a customized file exists, the new functions are added onto the menu bar under the name “v6.000”. Move functions to appropriate positions by looking at default positions shown on the next pages.



## **Menu bar parameter added**

### Board Designer PC board Outline Edit Module

- (View ) Component Origin
- (Utility ) Delete the component library on the PC board

### Board Designer Floor Plan Module

- (View ) Component Origin
- (Attribute Lock Component ) Reference
- (Attribute Unlock Component ) Reference
- (Utility ) Error List
- (Utility ) Delete the component library on the PC board
- (Utility ) Cursor Information Dialog Box
- (Module ) HIC

### Board Designer Placement/Wiring Module

- (Edit ) Template Placement/Wiring
- (View ) Component Origin
- (Attribute Lock Component ) Reference
- (Attribute Unlock component ) Reference
- (Utility ) Cursor Information Dialog Box
- (Utility ) Rebuild Electrical Net
- (Utility ) Check Surface
- (Utility ) Panel Data Display
- (Utility ) Error List
- (Utility ) Land Status Normalization Dialog Box
- (Utility ) Delete the component library on the PC board
- (DRC ) General DRC
- (Module Package ) BGA - F input/output
- (Module Package ) Bond Shell
- (Module Package ) Output Bond Shell
- (Module Package ) Output List
- (Module Package ) Delete Via-in-Via Error
- (Module Package ) Package DRC
- (Module Package ) DRC Mode
- (Module Package ) Error Mark Display
- (Module ) Direct Rambus
- (Module ) HIC

### Board Producer Artwork Module

- (View ) Component Origin
- (Utility ) Hole Drawing
- (Utility ) Delete the component library on the PC board
- (Utility ) General 2-D Icon
- (Utility Symbol Mark Design ) Symbol Mark Attribute Check

### Board Producer Manufacturing Panel Design Tool

- (View ) Component Origin
- (View ) Reference
- (Utility ) Delete the component library on the PC board
- (MRC ) Reference Overlap Check

# 1-13 User Font



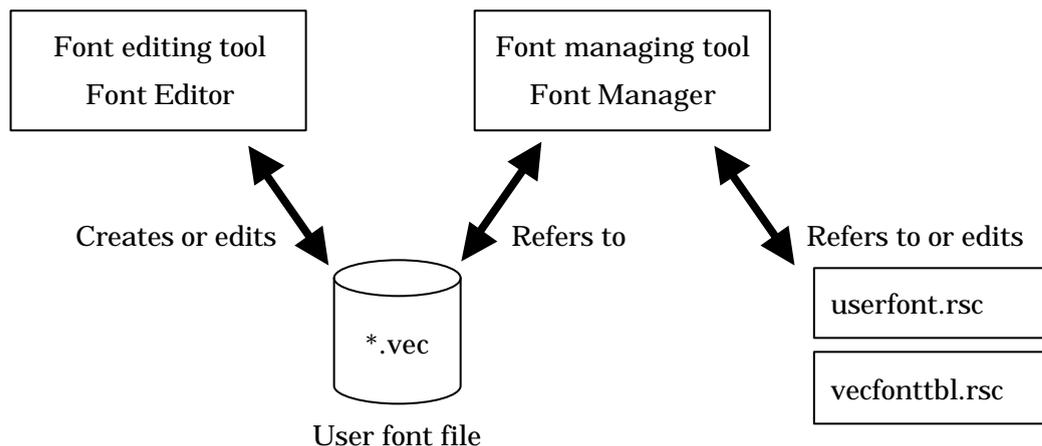
Rev. 6.0 supports user fonts.

- User font
- Font editing tool (Font Editor)
- Font managing tool (Font Manager)
- PWS user font conversion

## ● User font

### [Function]

The Rev. 6.0 CR-5000 CDB, BD and BP support user fonts. By employing user fonts, you can use a specific-shaped character in the PC board or component file.



The font editing tool (Font Editor) and font managing tool (Font Manager) are used to perform the following operations necessary to use a user font.

- Prepare a user font file.
- Allocate a font ID to the user font.
- Set the user font in the font combination table.

To use the user font used on the PWS on the CDB, BD or BP, convert it by using the PWS User Font Conversion Tool.

### Reference

To use user fonts on the System Designer, see “CR-5000 User’s Guide/6.3.3 User font operations (for SD).”

## ● Font editing tool (Font Editor)

### [Function]

This is the tool to create or edit a user font file used in the SD, CDB, BD and BP (.vec).

You can store user font files created with the font editing tool in the following two directories.

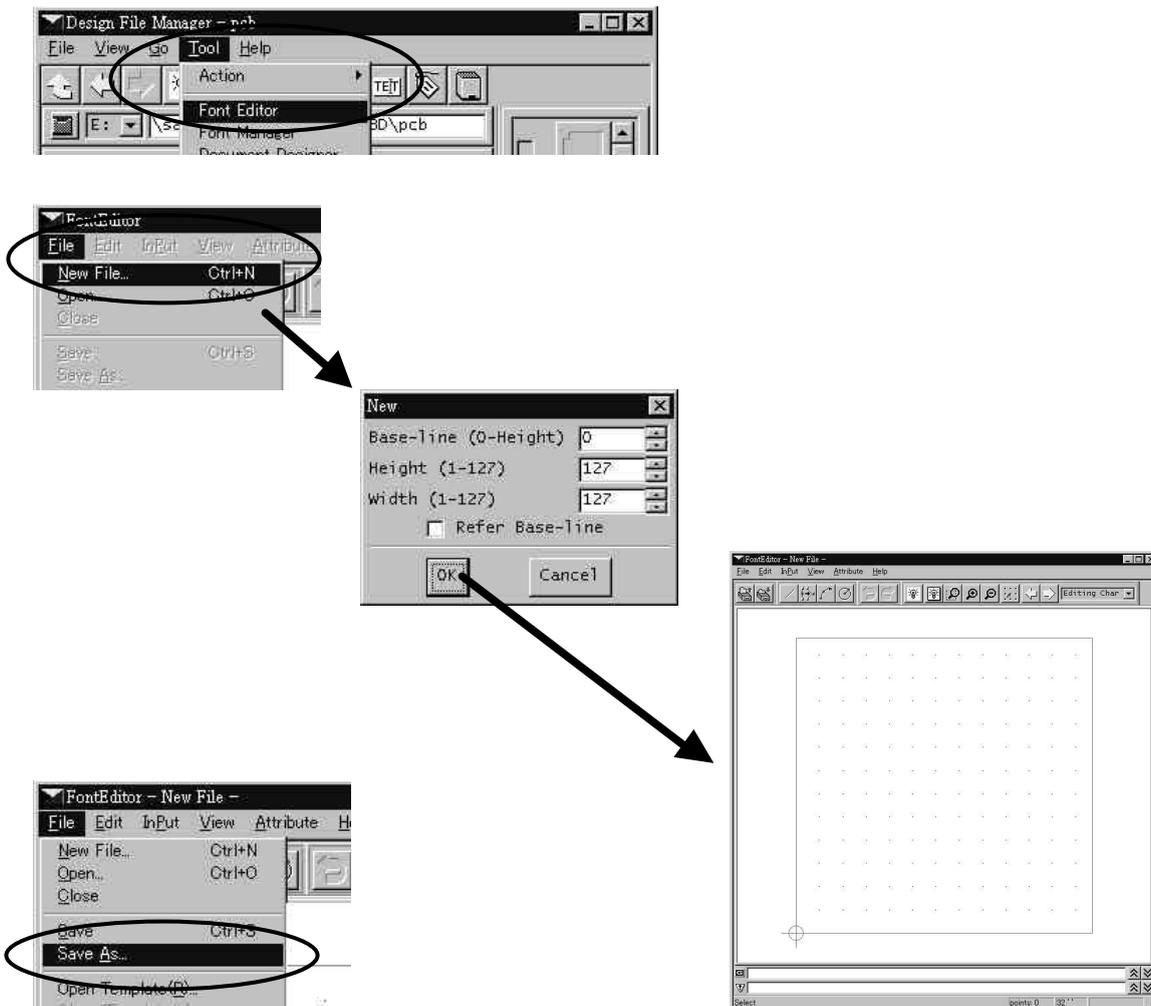
<Directory storing user fonts>

- (1) \$SCR5\_PROJECT\_ROOT/local/zsys/font/user/
- (2) \$ZLOCALROOT/zsys/font/user/

If both of the directories contain the file, the reference priority is (1) (2).

### [Operation]

- (1) Select **Tool** **Font Editor** from the Design File Manager menu bar.
- (2) Select **File** **New File..** from the Font Editor menu bar.
- (3) Click **OK** in the New dialog box.
- (4) After inputting or editing, select **File** **Save As...** from the Font Editor menu bar.



## ● Font managing tool (Font Manager)

This is the tool to copy font files or edit resource files in order to use the created user font file (.vec) on CDB, BD or BP.

- Allocating a font ID to the user font
- Setting the user font in the font combination table

### Allocating a font ID to the user font

#### [Function]

The font ID has information on “which character in the design data employs which font.” Therefore, you need to allocate an individual font ID to each user font file.

Correspondence between the font files and font IDs is managed by the following resource files.

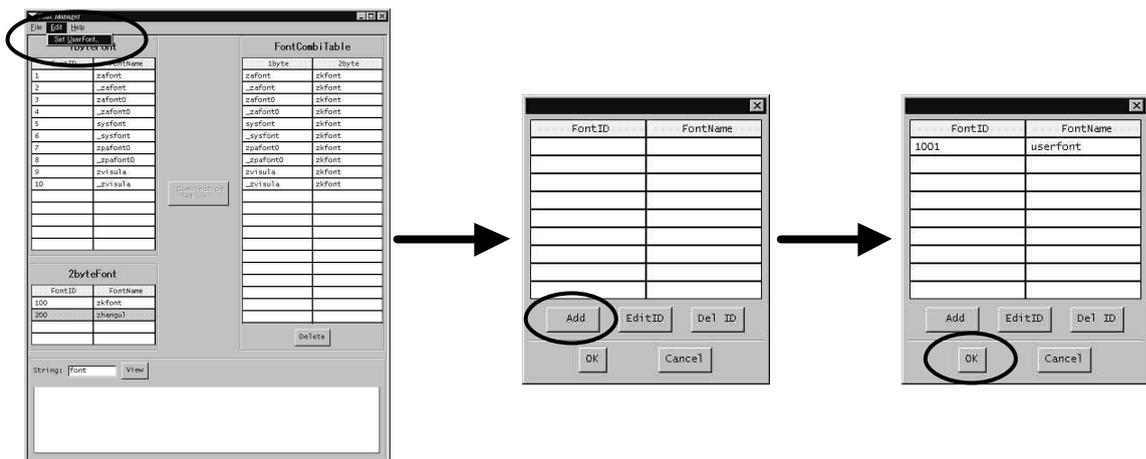
<userfont.rsc >

- |                                                    |
|----------------------------------------------------|
| (1)\$CR5_PROJECT_ROOT/local/zsys/info/userfont.rsc |
| (2)\$ZLOCALROOT/zsys/info/userfont.rsc             |

If both of the directories have this information, the reference priority is (1) (2).

#### [Operation]

- (1) Select **Tool** **Font Manager** from the Design File Manager menu bar.
- (2) Select **Edit** **Set User Font** from the Font Manager menu bar.
- (3) Click **Add** and specify a prepared user font.
- (4) Click **OK**.



#### [Notes and Restrictions]

- Because the Font Manager edits font ID allocation, or the “userfont.rsc” file, you do not need to pay attention to the internal format.

# **Setting the user font in the font combination table**

## **[Function]**

The CDB, BD and BP interactive design tools allow you to select a font from the “font combination table” for character input. The user font to be used must be included in the “font combination table.”

The “font combination table” is managed by the following resource files.

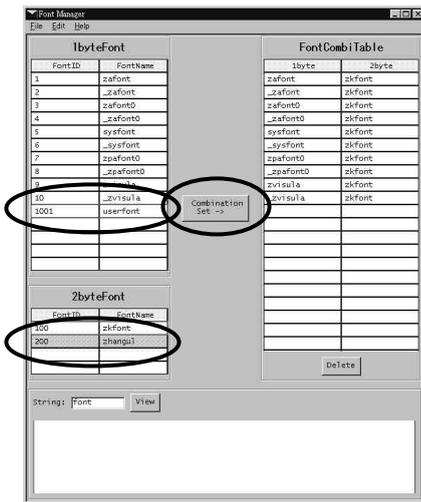
<vecfonttbl.rsc>

- (1) \$HOME/cr5000/ue/vecfonttbl.rsc
- (2) \$CR5\_PROJECT\_ROOT/zue/info/vecfonttbl.rsc
- (3) \$ZUEROOT/info/vecfonttbl.rsc

If multiple directories have this information, the system searches for the information in order from (1) (2) (3), referring to the file data first found.

## **[Operation]**

- (1) After allocating a font ID to the user font, select the added user font ID from the 1-byte font table on the Font Manager.
- (2) Select a font ID (100 for Japanese) from the 2-byte font table on the Font Manager according to your language environment.
- (3) Click **Combination Set ->**.
- (4) After inputting and editing, select **File Save the Font Combination Table** from the Font Manager menu bar.
- (5) After selecting the environment to save in the Save Font Combination Table dialog box, click **OK**.



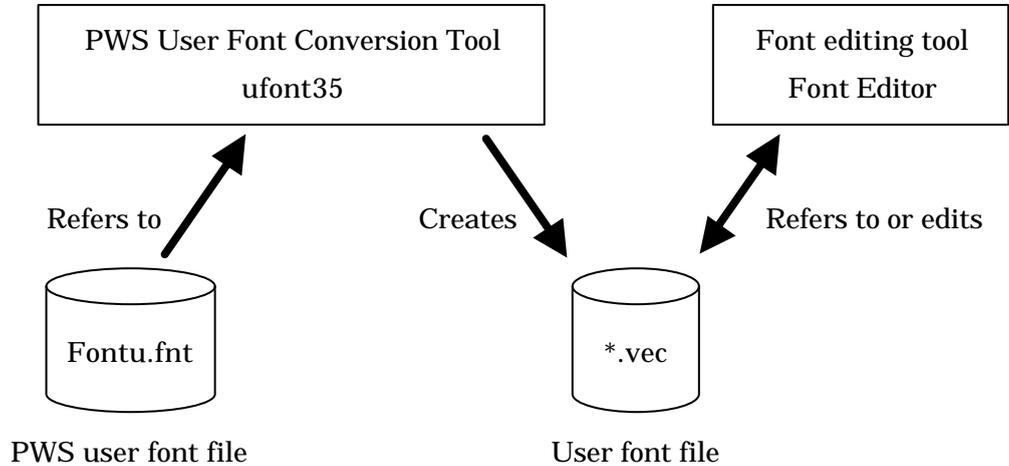
## **[Notes and Restrictions]**

- Because the Font Manager adds data to and updates the font combination table, or edits the “vecfonttbl.rsc” file, you do not need to pay attention to the internal format.

## ● PWS user font conversion

### [Function]

With Rev. 6.0, you can convert user fonts used with the PWS to user fonts that can be used on CDB, BD or BP by using the PWS User Font Conversion Tool.



### [Operation]

To start the PWS User Font Conversion Tool (ufont35), enter the following.

```
ufont35.sh Required parameter [Optional parameter]
```

\* On the Windows-version, use ufont35.exe for activation.

#### Required parameter

**-r PWS user font path name**

Path for the PWS user font file to convert.

**-o BD user font path name**

Path for BD user font file created after conversion.

**-p:font PWS user font font number specification**

Specifies the font number that converts the font in the PWS user font from 1 to 8.

#### Reference

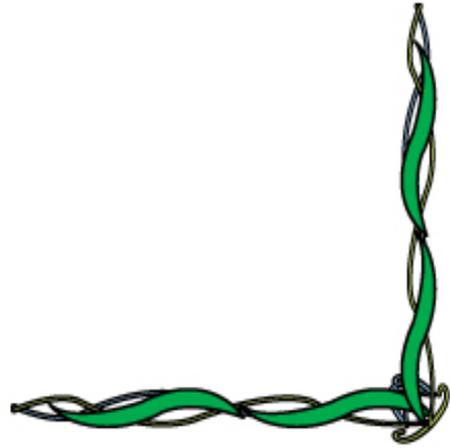
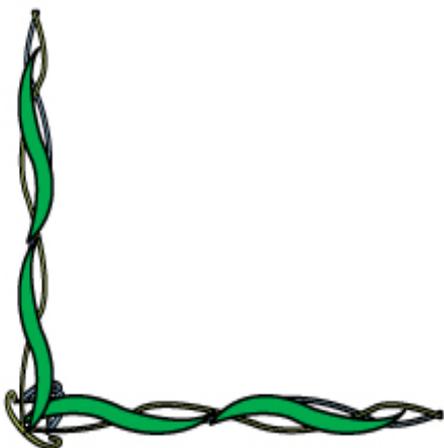
For optional parameters, see “CR-5000 User’s Guide/6.3.4 Using the PWS user font.”



# **Chapter 2**

## **Components Manager**

### **(CDB)**



# 2-1 Added Root Menu Functions



With Rev. 6.0, the following functions are added or improved for the Components Manager root menu.

- CDB tree view
- New registration of an object from the root menu

## ● CDB tree view

The CDB tree view function displays objects registered in the part, package or footprint library in tree structure on the Components Manager root menu.

- Displaying objects in tree structure
- Executing an action for an object

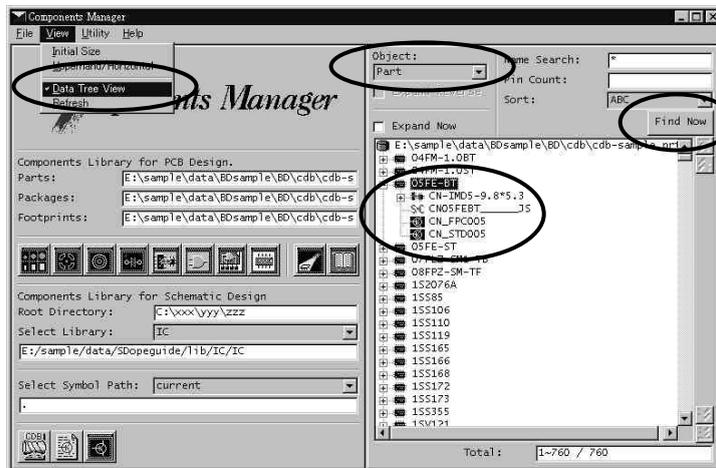
### Displaying objects in tree structure

#### [Function]

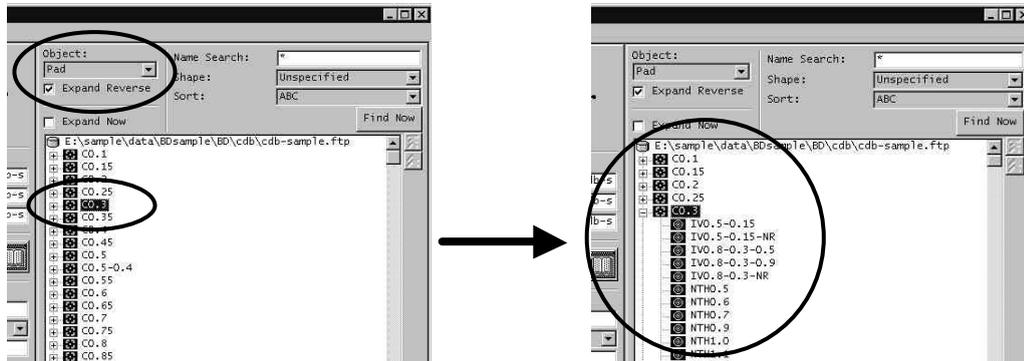
This function displays objects in the library in tree structure, enabling you to see relationships between objects at a glance.

#### [Operation]

- (1) Select **View** **Data Tree View** from the Components Manager menu bar to display the tree view area on the right of the root menu.
- (2) Selecting [Object] or clicking **Find Now** displays objects in tree structure.
- (3) Double-clicking the tree item in the tree view area or clicking [+] on the left breaks down the related subordinate objects.



- (4) Select Pad for [Object].
- (5) Select the [Expand Reverse] check box.
- (6) Double-clicking tree item in the tree view area or clicking [-] on the left breaks down the related parent object.



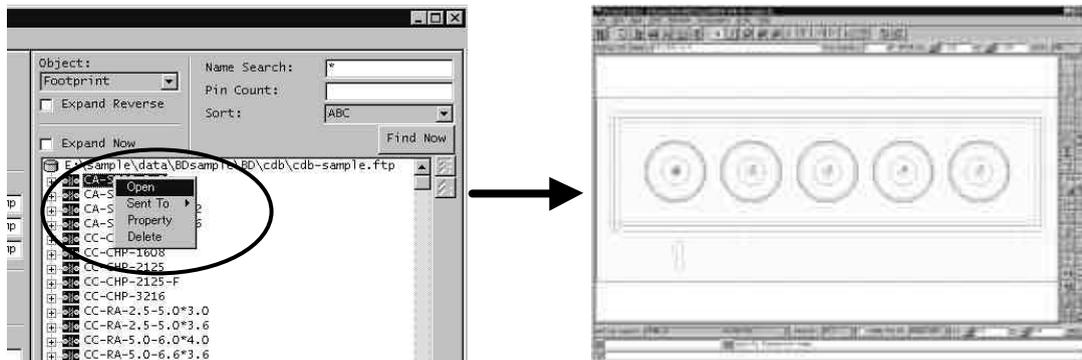
## **Executing an action for an object**

### **[Function]**

You can directly start the editing tool or utility function related to a selected object, delete the selected object or refer to the user-defined attribute.

### **[Operation]**

- (1) Select a tree item in the tree view area and right-click.
- (2) Select **Open** on the Assist Menu.
- (3) Start the registration tool corresponding to the selected object.



### **[Notes and Restrictions]**

- You cannot select multiple tree items, move them, change their names and drag and drop them.
- You cannot display the property of a schematic symbol.
- You cannot delete schematic symbols and stock codes.
- It may take some time to break down the subordinate objects for a pad or padstack in the tree structure in the Expand Reverse or Expand Now mode object, when the reference relationship with the parent object is complicated.

## ● New registration of an object from the root menu

### [Function]

With Rev. 6.0, you can choose to create an object by selecting **File** **New** from the Components Manager menu bar.



# 2-2 Utility Tools



The following functions are added or improved.

- Object Comparison Tool
- Attribute Table Registration Tool

## ● Object Comparison Tool

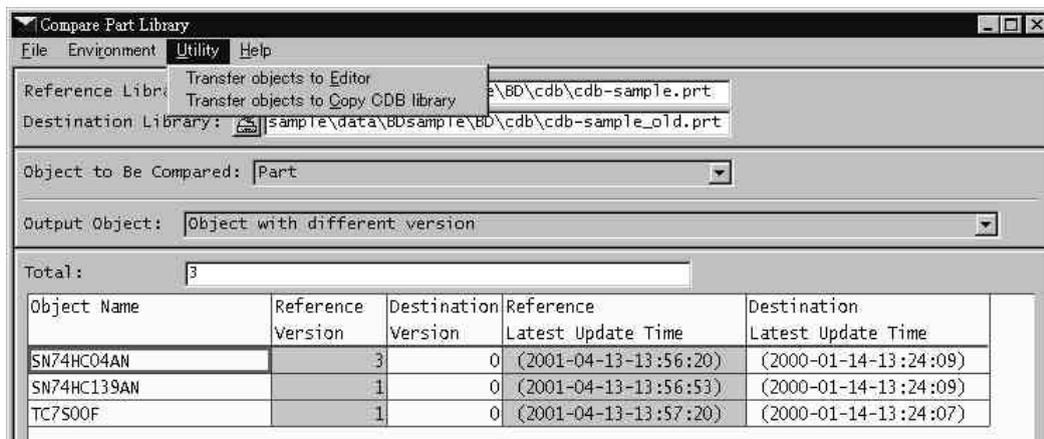
### [Function]

For example, if you transport libraries between multiple offices during PC board design operation, you may want to check differences between the CDB for the library supplier and that for the PC board designer.

With Rev. 6.0, you can compare libraries and extract objects with different information. You can also transfer extracted objects to the Copy Tool or Registration Tool.

### [Operation]

- (1) Select **Utility** **Compare Objects** from the Components Manager menu bar.
- (2) Select a reference library, destination library, object to be compared and those to output.
- (3) Select **Execute**.
- (4) To transfer extracted objects to the Registration Tool, select **Utility** **Transfer objects to Editor**.  
To transfer extracted objects to the Copy Tool, select **Utility** **Transfer objects to Copy CDB library**.



## ● Attribute Table Registration Tool

The following improvements and additions were made on the Attribute Table Registration Tool.

- Increased objects to edit
- Updating displayed data to the latest information
- Specifying an object to display
- Batch setting of attributes to multiple objects
- Improved data saving

### **Increased objects to edit**

#### **[Function]**

With Rev. 6.0, you can edit the following six component objects in addition to the conventional parts and stock codes.

- Pin assignment
- Function
- Package
- Footprint
- Padstack
- Pad

#### **[Notes and Restrictions]**

- As objects to be edited are added, if the part, package or footprint library cannot be opened in the editing mode upon tool activation, you cannot display the option list used to select an object to be edited.

### **Updating displayed data to the latest information**

#### **[Function]**

With Rev. 5.0 or older, you cannot refer to updated information on the table even if another tool or user updates database information after you have selected an object until **Reset** or **Save** is selected.

With Rev. 6.0, you can load the latest information database at any time and reflect it to table display.

However, unless data is saved, the cell display is not updated.

#### **[Operation]**

Select **View** **Refresh** from the menu bar.

## Specifying an object to display

### [Function]

While Rev. 5.0 displayed all objects registered in the database on the table, Rev. 6.0 is able to display only the objects with the attributes satisfying specified rules.

### [Operation]

Edit the third label row for each attribute and specify a character string.

Object: Package

Package Name	Package Type	therm.
&id	&packageType	
*	DIP	
IC-DIP8-300	DIP	
IC-DIP14-300	DIP	
IC-DIP16-300	DIP	
IC-DIP18-300	DIP	

Cells on the third label row

### [Notes and Restrictions]

- You can use regular expressions (\*, ?, [ ]) in character strings.
- Upper-case and lower-case characters are differentiated, (case-sensitive).
- Integer or real number type attributes are regarded as character strings for comparison.

## Batch setting of attributes to multiple objects

### [Function]

With Rev. 6.0, you can specify a value to an editable attribute and set it to all objects displayed in the table in a batch.

### [Operation]

- (1) Double-click the cell on the first or second label line of column to which you want to set the attribute.
- (2) Set a value with the dialog box corresponding to the column attribute and select **OK**.

Object: Part

Part Name	# Of Pins	Package Name	Pin Assignment Name	schem
&id	&#pins	&packageName	&pinassignName	symbol
*	*	*	*	*

Cells on the first and second label rows

## **Improved data saving**

### **[Function]**

With Rev. 5.0, all edited data was not reflected in the database if an error occurred during saving.

Rev. 6.0 reflects edited cells for which no error occurred in the database on data saving.

Note that the cell background not reflected in the database is red.

Part Name &id *	# of Pins &#pins *	Package Name &packageName *	Pin Assignment Name &pinassignName *	schematic symbol name symbolName1 *
04FM-1.0BT	4	CN-IMD4-6.0*4.4	7400	CN_FPC004
04FM-1.0ST	4	CN-TMD4-7.6*6.0	7400	CN_FPC004
05FE-BT	5	Cr	DATA TEMP#CR516.acerr	
05FE-ST	5	Cr	File	
07FLZ-SM1-TB	7	Cr		
08FPZ-SM-TF	8	Cr		
1S2076A	2	D-		
1SS85	2	D-		

ERROR: Cannot find 7400.  
Object "04FM-1.0BT", Attribute "Pin Assignment Name"  
ERROR: Cannot find 7400.  
Object "04FM-1.0ST", Attribute "Pin Assignment Name"

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## 2-3 Added Functions Common to CDB

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The following functions are added or improved for Rev. 6.0.

- Displaying the confirmation dialog box upon object saving
- Automatic updating of Search dialog box upon object saving eliminated
- Function to overwrite when saving data under another name
- Outputting table display to a file
- Expanded arbitrary command argument

### ● Displaying the confirmation dialog box upon object saving

#### [Function]

Rev. 5.0 saved an object at the specified time.

Rev. 6.0 can display the confirmation dialog box before saving as the BD. If you specify “ON” in the resource file for each registration tool, the confirmation dialog box appears.

#### [Notes and Restrictions]

- The Part, Package, Pin Assignment, Function, Pad Canvas, Padstack and Footprint Registration Tools support this function.
- If the keyword is omitted or data other than “ON” is specified, the default is OFF.

#### Reference

For resource files, see “1-4 List of Changed Resource Files ?\$ZCSROOT/info/XXX.rsc.” (XXX: SPart, Package, Pinassign, Function, Footprint, Padstack or Pad)

### ● Automatic updating of Search dialog box upon object saving eliminated

#### [Function]

Rev. 5.0 automatically updated the list when the object being edited with the registration tool was saved and the object search dialog box was displayed.

However, automatically updating the list when an object is saved is not that helpful and can degrade efficiency. Therefore, this function is eliminated in Rev. 6.0.

You can update the list at any time by selecting **View** **Refresh** from the menu bar for each Search dialog box.

## ● Function to overwrite when saving data under another name

### [Function]

When trying to execute **Save As...** with the Pad Canvas, Padstack or Footprint Registration Tool, Rev. 5.0 outputs an error and interrupted the process if the specified object name existed.

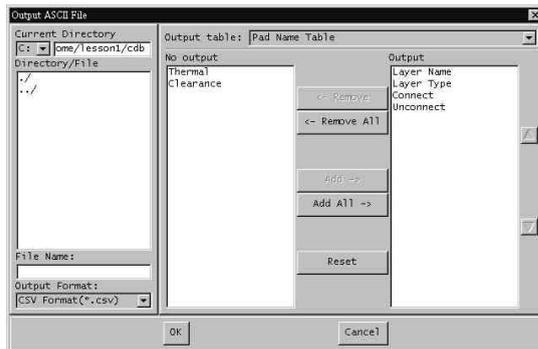
Rev. 6.0 displays the confirmation dialog box for overwriting. You can overwrite data by clicking **OK**.

## ● Outputting table display to a file

### [Function]

When outputting data displayed in table format with a registration tool such as the Padstack Registration Tool to a file, you could only specify the output destination filename and output format with Rev. 5.0.

With Rev. 6.0, you can also specify columns to output and change the order of columns in the file on each tool.



### [Operation]

- (1) Select **File** **ASCII File Output** on the menu bar for each tool.
- (2) If an item that you do not want to output is in the [Output] field, select **Remove** or double-click it to move it to the [No output] field.
- (3) When you do not want to output all columns, click **Remove All**.
- (4) After specifying columns to output, click **OK**.

### [Notes and Restrictions]

- The Padstack Registration Tool requires different operations for outputting the [Pad name] table and the [hole shape] table to files.

Therefore, to save data displayed in both tables to a file, as with Rev. 5.0 or older, follow the directions below.

- (1) Output data in each table to different files: pad.csv and hole.csv.
- (2) Merge two files by using cat and other commands.

Example) %cat pad.csv hole.csv >both.csv

## ● Expanded arbitrary command argument

### [Function]

Rev. 6.0 can pass opened data name to an arbitrary command (by selecting **Utility** **Arbitrary Command** from the menu bar). Some keywords are provided in addition to data names to pass on a variety of information.

#### <New keyword list>

Keyword	Description	Tool name that supports the keyword			
		(*1)	(*2)	LCDB extraction	Data consistency batch check
\$zcs_data_name	Opened data name	?	×	×	×
\$zcs_data_type	Opened or targeted data type. (part, pinassign, function, package, footprint, padstack or pad)	?	?	?	?
\$zcs_db_path	Library path to be edited	?	?	?	×
\$zcs_prtdb_path	Reference part library path	?	?	?	?
\$zcs_pkgdb_path	Reference package library path	?	?	×	?
\$zcs_ftpdb_path	Reference footprint library path	?	?	×	?
\$zcs_tool_name	Started tool name	?	?	?	?
\$zcs_version	Data version number	?	×	×	×
\$zcs_user_name	Data editor name	?	×	×	×

? : Supported

× : Not supported

\*1: Part registration, pin assignment registration, function registration, package registration, footprint registration, padstack registration and pad canvas registration

\*2: Pad table registration, attribute table editing, CDB library copying, CDB library purging, generic part generation, object batch deletion

### [Notes and Restrictions]

● New keywords are available with the CDB Registration Tool only.

The Design File Manager and other tools do not support them.

#### Reference

For details on utilization and restrictions, see online help for CDB Arbitrary Command dialog box.

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# 2-4 Part Library-Related Functions

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The following functions are added or improved for the Part Library Registration Tool.

- Improved schematic symbol pin information loading
- Automatic setting function for pin names
- Comment input on unadmitted part registration

## ● Improved schematic symbol pin information loading

### [Function]

When you select a symbol from the Symbol Search dialog box or directly input a symbol name in the table during function registration, pin information registered as the symbol data is loaded to the pin table.

Rev. 6.0 sorts information in ascending order by using symbol pin IDs that every symbol has when loading symbol data pin information to realize an easy-to-see array.

## ● Automatic setting function for pin names

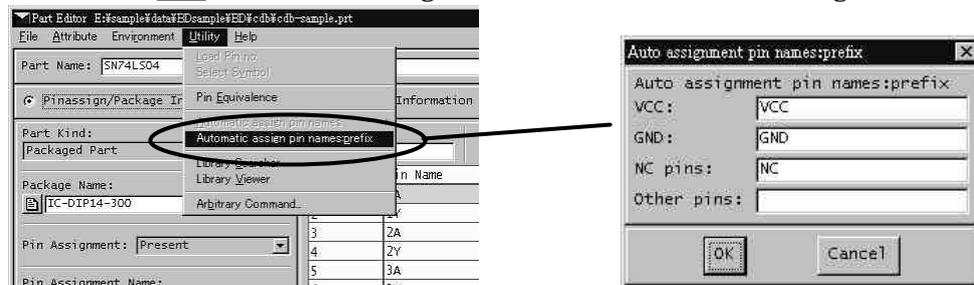
### [Function]

With Rev. 5.0, when the number of pins was specified as 2 while registering part and pin assignment, “A” and “B” were automatically allocated as pin names.

In such a case, pin names are not set with Rev. 6.0. When you set pin names to be automatically allocated, the pin number or the pre-set prefix plus the pin number is set as the pin name.

### [Operation]

- (1) Select **Utility** **Automatic assignment pin names: prefix**.
- (2) Specify a prefix with the started Auto Assignment Pin Names: Prefix dialog box.
- (3) Select **OK** in the Auto Assignment Pin Names: Prefix dialog box.



## ● Comment input on unadmitted part registration

### [Function]

With Rev. 6.0, you can use input comments by using GUI at unadmitted part registration.

### [Operation]

- (1) Select whether this is the admitted part (Yes or No) in the Admitted Part Setup area for the Part Registration Tool.
- (2) When the admitted part attribute is set to [No], the field below becomes active. Input a comment.
- (3) To select one of the reasons with the list icon, pre-define them in the resource file (part.rsc).
- (4) The comment set in the [Reason] field is automatically set as the user-defined attribute, [reasonForUnauthorization] when the data is saved.

admission	NO
reasonForUnauthorization	Solder method is not determined.

### [Notes and Restrictions]

- The user attribute, [reasonForUnauthorization], which indicates the reason for not admitting the part, is deleted when the data is saved as the admitted part (i.e. [Yes] is selected for the [Admitted Part] attribute).
- When data is saved after directly editing and changing the user attribute, [Admission] in the User Attribute Setup dialog box, the comment set in the user attribute, [reasonForUnauthorization] is not deleted.

## 2-5 Enhanced Figure — Editing Function for Footprint



The following functions are now available for the Rev. 6.0 registration tool for the footprint library.

- Loading data to another footprint
- Inputting a figure to another footprint
- Function to input offset figures added
- Function enhanced to input and edit dimension lines
- Limit on inputting characters on a conductive layer eliminated
- Function added to input and delete windows (Pad canvas registration)

### ● Loading data to another footprint

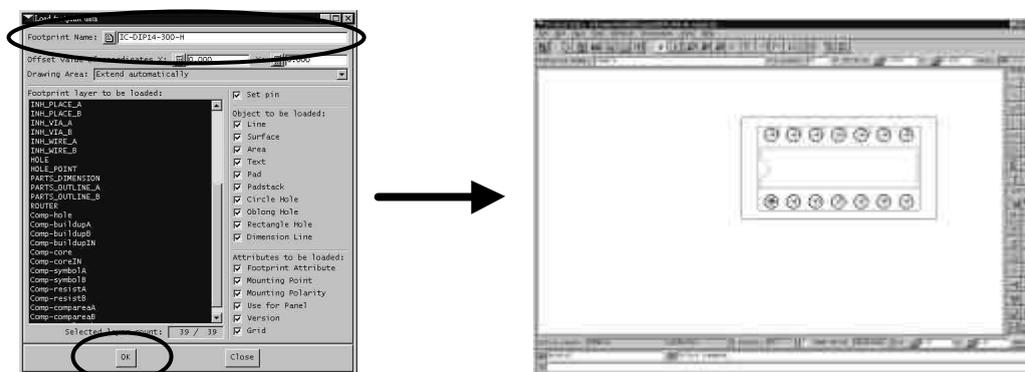
#### [Function]

Rev. 6.0 has a new function to load data defined in another footprint, such as figure and attribute information, to the footprint being edited using the Footprint Registration Tool.

This enables easy use of registered footprints as a template and considerably saves you the time and work in registering component information in the CDB.

#### [Operation]

- (1) Select **File** **Load** from the Footprint Registration Tool menu bar.
- (2) Set parameters such as footprint name in the started dialog box.
- (3) Clicking **OK** at the bottom of the dialog box loads data such as figure and attribute information defined in the footprint according to set parameters.



#### [Notes and Restrictions]

- While objects input in the footprint layer that are not set as visible layer are loaded (considered during drawing area calculation), they are not displayed.

## ● Inputting a figure to another footprint

You can input figure information to another footprint such as line and padstack into arbitrary coordinates by dragging as if you were using the padstack input or pad input command. This command can load only figure information and is different from the function explained in “Loading data to another footprint” above. However, this function enables subsequent input of figures by dragging them and, therefore, is useful in loading data from a footprint defining part of a component shape, such as the shape around a pin.

- Inputting a figure to another footprint
- Selecting a layer to load
- Selecting an object to load

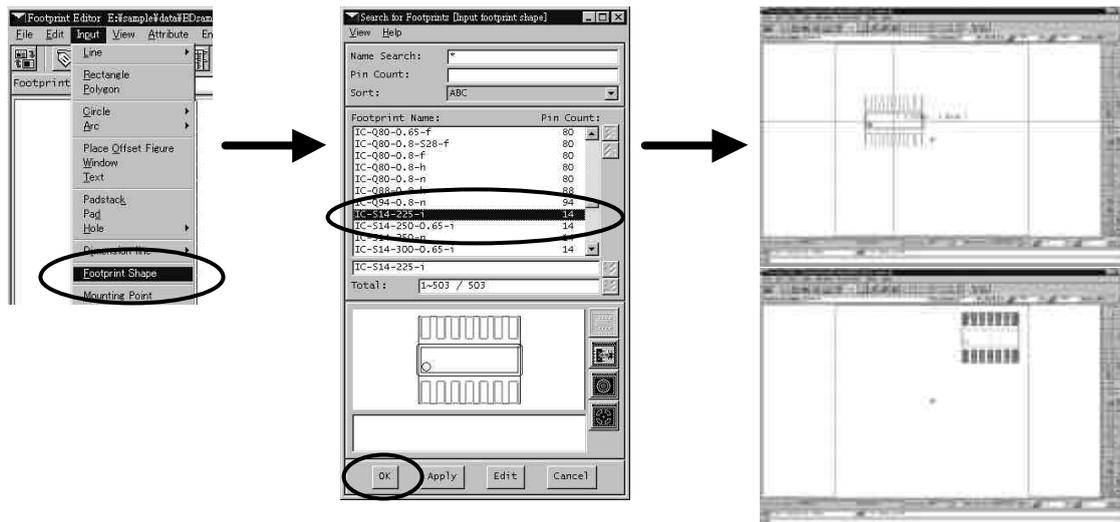
## Inputting a figure to another footprint

### [Function]

This function inputs figure information input in another footprint into arbitrary coordinates by dragging.

### [Operation]

- (1) Select **Input** **Footprint Shape** from the Footprint Registration Tool menu bar.
- (2) Specify a footprint name to be loaded to the started Search for Footprints dialog box.
- (3) Click **OK** at the bottom of the dialog box drags the specified footprint.
- (4) Specify a position on the canvas or coordinates to input.



### [Notes and Restrictions]

- While objects input to the footprint layer that are not set as visible layer are loaded (considered during drawing area calculation), they are not displayed.

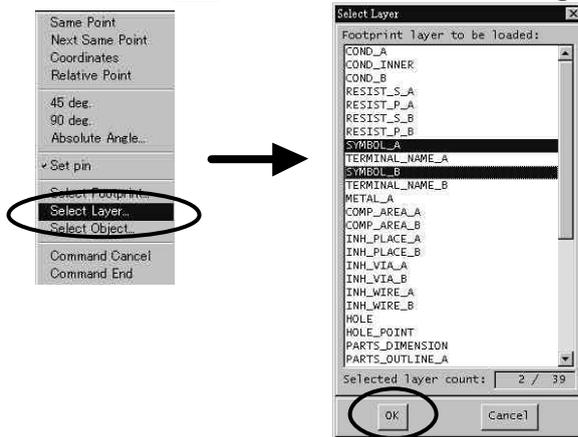
## Selecting a layer to load

### [Function]

You can specify a footprint layer to load when inputting a footprint.

### [Operation]

- (1) Right-click the mouse while dragging a footprint.
- (2) Click **Select Layer...** in the started Assist Menu.
- (3) Specify a footprint layer to load in the started Select Layer dialog box.
- (4) Click **OK** at the bottom of the dialog box.



### [Notes and Restrictions]

- Padstacks are loaded regardless of layer specification. To leave padstacks unloaded, see the next section, "Selecting an object to load".

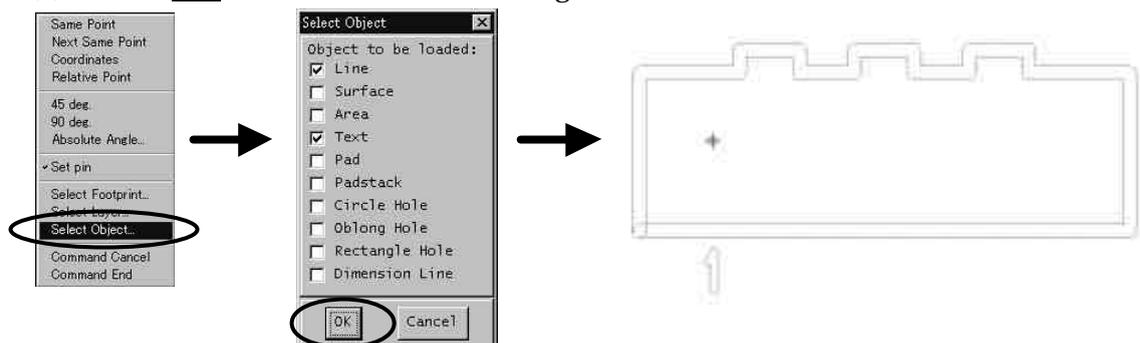
## Selecting an object to load

### [Function]

You can specify an object to load when inputting a footprint.

### [Operation]

- (1) Right-click the mouse while dragging a footprint.
- (2) Click **Select Object...** in the started Assist Menu.
- (3) Specify a footprint object to load in the started Select Object dialog box.
- (4) Click **OK** at the bottom of the dialog box.



## ● Function to input offset figures added

The following functions are added for the Rev. 6.0 Offset Figure Input command to enhance the figure editing functions for the Footprint Registration Tool and Pad Canvas Registration Tool.

- Deleting reference figures
- Specifying a base position for lines at offset input
- Adding an offset reference and an offset figure

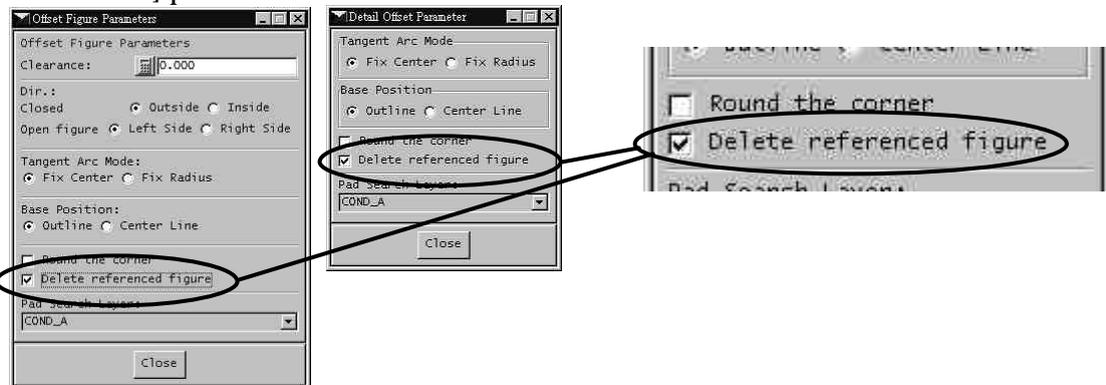
### **Deleting reference figures**

#### **[Function]**

With Rev. 6.0, you can delete the offset reference figure when generating an offset figure.

#### **[Operation]**

- (1) Select **Input** **Input Offset Figure** from the menu bar.
- (2) Select the **[Delete referenced figure]** check box in the sub-dialog box or the **[Set Detail]** panel menu.



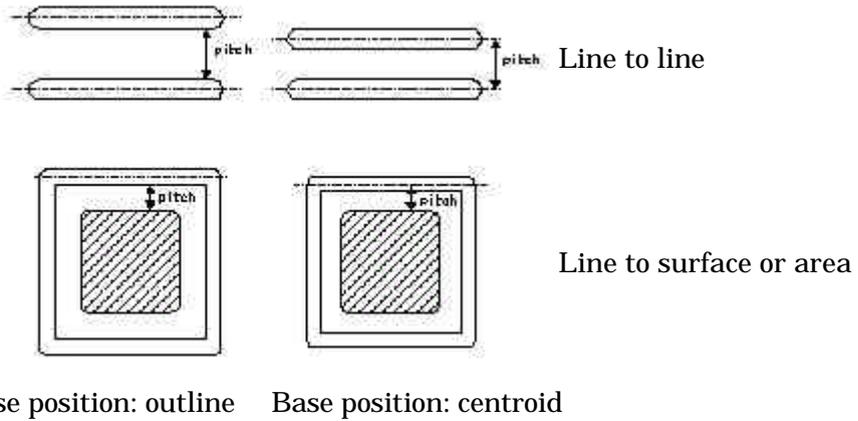
#### **[Notes and Restrictions]**

- If the offset reference figure is pad, padstack or figure set as pin, it is not deleted.

# Specifying a base position for lines at offset input

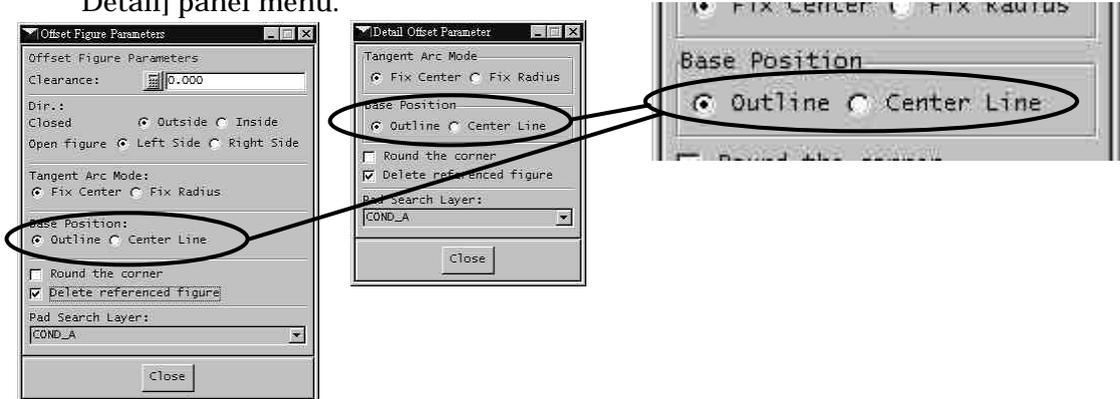
## [Function]

With Rev. 6.0, you can select a base position for pitch at offset: outline of line or centroid.



## [Operation]

- (1) Select **Input** **Input Offset Figure** from the menu bar.
- (2) Select an option button in [Base Position] in the sub-dialog box or the [Set Detail] panel menu.



## [Notes and Restrictions]

- While Rev. 5.0 used the line centroid as a reference by default to generate surfaces, Rev. 6.0 uses the outline as the default line base position. Note that the function is different.

## Adding an offset reference and an offset figure

- You can generate lines for a surface or area.
- You can specify a pad to generate a surface, area or line.

## ● Function enhanced to input and edit dimension lines

### [Function]

The following parameters, which can be set upon input, are added for the Rev. 6.0 dimension line input function. In addition, the GUI for this function is unified with the BD and BP dimension line input GUI, enabling the same editing operations.

#### <Function enhancement related to the input function>

- User-defined specification of the dimension line type
- Intersecting character strings
- Font specification
- Character for the dimension character offset
- Arrow shape specification for character extraction
- Auxiliary line use specification
- Dimension line type specification
- Angle for character extension
- Size specification with the character table
- Character reference point specification
- Vertexes and nearest point specification
- Dimension line arrow shape specification
- Arrow direction specification
- Setting a dimension value for the dimension value type (leading line)
- Extraction at a free angle
- Input by double-clicking
- Specifying a character position with coordinates with text leading line

#### <Function enhancement related to the edit function>

- Moving a dimension character string
- Changing the arrow direction
- Extending and shortening an auxiliary line
- Extending and shortening a dimension line
- Tolerance character string use specification
- Changing the character angle
- Changing the arrow shape
- Specifying Auxiliary line use specification
- Text leading line use specification

### [Notes and Restrictions]

Rev. 6.0 does not support dimension character string editing by inputting a canvas key.

## ● Limit on inputting characters on a conductive layer eliminated

### [Function]

With Rev. 6.0, you can input characters onto the conductive layer while registering a footprint.

## ● Function added to input and delete windows (Pad canvas registration)

### [Function]

The Window Input and Delete commands are added for the Rev. 6.0 Pad Canvas Registration Tool.

# 2-6 Footprint — Parametric Registration



The following functions are added or improved.

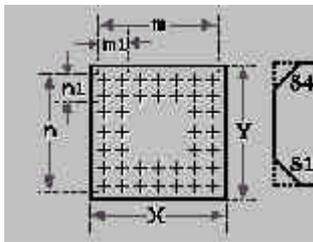
- Added PGA shape generation parameter
- Expanded function to load the pin coordinate table
- Added DIP/SOP shape generation parameter
- Added connector/ZIP shape generation parameter

## ● Added PGA shape generation parameter

### [Function]

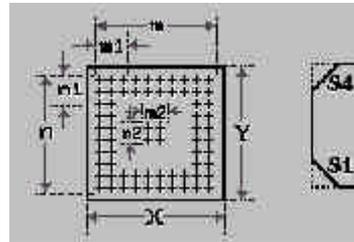
In Rev. 6.0, the table cell used to set the parameter for the number of center ball pins (m2,n2) is added and icon appearance is changed, enabling automatic generation of center balls. The tool resource file (footprint.rsc) and parametric resource file (figure.rsc) formats are also changed in line with the added parameter.

Rev.5.0



Number of Terms m	m	14
Number of Terms m1	m1	3
Number of Terms n	n	14
Number of Terms n1	n1	3

Rev.6.0



Cut Surface 4	S4	0
Number of Terms m	m	14
Number of Terms m1	m1	3
Number of Center Terms m2	m2	3
Number of Terms n	n	14
Number of Terms n1	n1	3
Number of Center Terms n2	n2	3
Term Pitch x		2.54

### [Operation]

- (1) Click **Utility** **Parametric Registration** on the menu bar, and then select [Generate PGA shape].
- (2) Input the number of center balls to be automatically generated in the [m2] and [n2] fields in the parameter dialog box.

## ● Expanded function to load the pin coordinate table

The following functions are expanded.

- Selecting the origin of component
- Supporting BGA format file parameter expansion

### Selecting the origin of component

#### [Function]

You can select [(0.0) of Pin coord. list] or [Center of a Component] as the component origin in [Loading the pin coordinate table].

- [(0.0) of Pin coord. list] (default):

Coordinates specified in the coordinate list are used to generate a pin shape and the coordinate (0.0) is used as the drawing origin.

- [Center of a Component]:

The center of minimum rectangle enclosing the generated pin shape is used as the drawing origin.



### Supporting BGA format file parameter expansion

#### [Function]

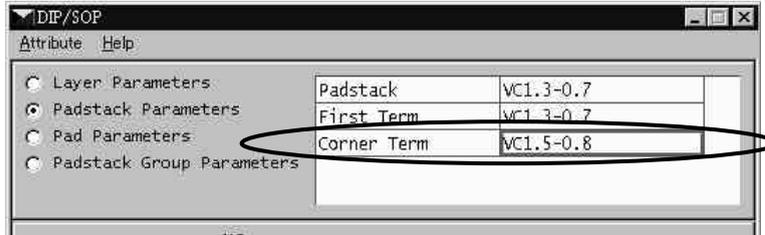
A function is added to select a ".ftp name" from the BGA format file (CSV file defining the pin position, shape and signal per component) if this file has multiple component shapes when loaded.



## ● Added DIP/SOP shape generation parameter

### [Function]

Parameters [Padstack parameter], [Corner Term] is added to [DIP/SOP shape generation]. This enables specification of another padstack to a corner pin other than Pin 1.



### [Notes and Restrictions]

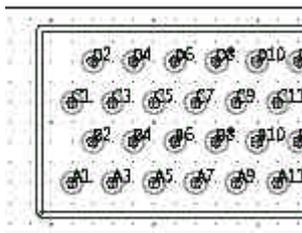
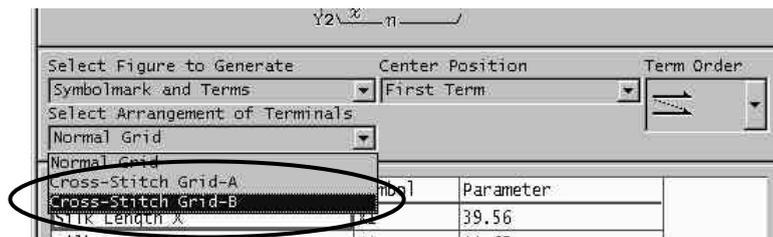
- To specify different padstacks for four corner pins, specify different padstack names in the [First Term] and [Corner Term] fields.

## ● Added connector/ZIP shape generation parameter

### [Function]

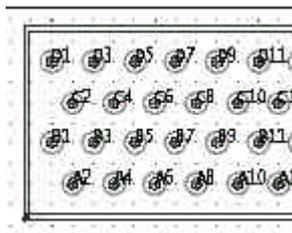
The cross-stitch pattern B is added as parameter [Select Arrangement of Terminal] for [Connector/ZIP shape generation]. When specified, the left-lowermost Pin 1 is placed further right than the left-most pin on the second line from the bottom.

Also, a mode is added to allocate numbers from the left-lowermost corner to the right in parameter [Term Order], with alphabetic and numeric pin numbers available for assignment.



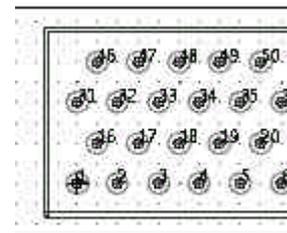
Cross-stitch A

Numeric pin number



Cross-stitch B

Numeric pin number



Cross-stitch A

Pin assignment: right to left

---

## 2-7 Footprint — Functions Related to Display

---



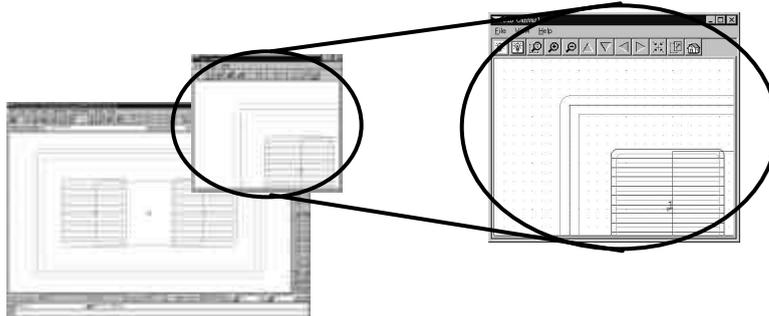
The following functions are added or improved for Rev. 6.0.

- Sub-canvas support
- Pin number display position specification
- Improved display

### ● Sub-canvas support

#### [Function]

With Rev. 6.0, you can use sub-canvases with each registration tool for the footprint library. This enables efficient operation when you want to refer to multiple points at the same time.



#### [Notes and Restrictions]

- If you open another data while keeping a sub-canvas displayed, the display areas in all sub-dialog boxes remain the same and data is redisplayed.
- Visible layers on each sub-canvas refer to the setting in the main dialog box.
- This does not support the window synchronization mode.
- The canvas split function for the Padstack Registration Tool has been replaced with this function.

#### Reference

For the number of windows that can be activated at the same time, see “1-4 List of Changed Resource Files ? \$ZCSROOT/info/footprint.rsc, ? \$ZCSROOT/info/padstack.rsc, ? \$ZCSROOT/info/pad.rsc.”

## ● Pin number display position specification

### [Function]

With Rev. 5.0, you could specify whether to display pin numbers.

With Rev. 6.0, you can also specify the reference point in displaying pin numbers.

### Reference

For defining this in the resource file, see “1-4 List of Changed Resource Files ?\$ZCSROOT/info/footprint.rsc.”

## ● Improved display

The following functions are improved.

- Improved cursor display
- Ruler rubber band display
- Automatic adjustment of column display width

### **Improved cursor display**

#### [Function]

The cursor shape is changed depending on the command status for the Rev. 6.0 Footprint and Pad Canvas Registration Tools, improving operability and realizing unification.

### **Ruler rubber band display**

#### [Function]

When you execute the ruler function on Rev. 6.0, you can display the ruler rubber band.

### **Automatic adjustment of column display width**

#### [Function]

Rev. 6.0 automatically adjusts display width of each column in the table. This facilitates displaying and checking of the entire object name.

---

## 2-8 Footprint — Improved Operability

---



The following functions are added or improved.

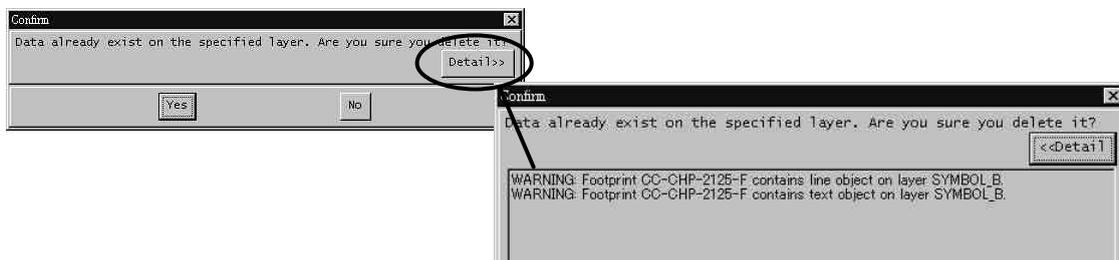
- Deleting footprint layers with input data
- Expanded object search rules
- Changing a padstack group name
- Matrix setting of user-defined the pin numbers in footprint.rsc
- Expanded automatic pin set function
- Pin coordinate list input/output
- Tabulating the grids, character sizes and pen widths
- Improved function related to the point specified at figure selection
- Unified coordinate input operation
- Warning message display at padstack saving
- Wire-bonding pad automatic generation pin parameter table [optional]

### ● Deleting footprint layers with input data

#### [Function]

With Rev. 5.0, you could not delete a footprint layer with input data. Therefore, if a layer with input data became unnecessary due to revision of the layer structure, deleting was cumbersome.

To solve this problem, we have revised Rev. 6.0 to delete such footprint layers. When you try to delete such a footprint layer, a confirmation dialog box appears so that you can select forcible deletion of the footprint layer (including data input on the layer).



#### [Notes and Restrictions]

- If the footprint is being edited or the footprint layer is being used by a padstack, just as with Rev. 5.0 or older, you cannot delete it.
- If the deleted footprint layer is being used in the technology library, modify the corresponding technologies.

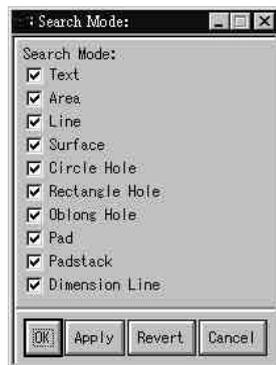
## ● Expanded object search rules

### [Function]

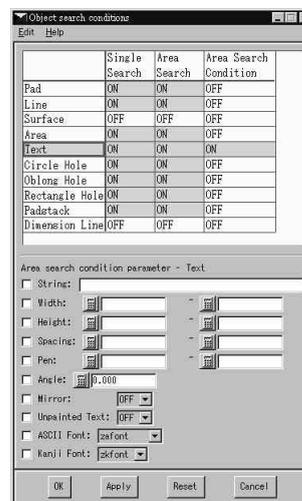
When you search an object in Rev. 6.0, you can specify the following rules per object type such as line, surface or pad.

- Single search target or not
- Area search target or not
- Area search rule
- Whether to validate the area search rule

Rev. 5.0



Rev. 6.0



### [Notes and Restrictions]

- Settings in the [Object search conditions] dialog box are referred to when the pin number automatic set command is executed.

## ● Changing a padstack group name

### [Function]

With Rev. 6.0, you can change a padstack group name.

### [Notes and Restrictions]

- You cannot change a default padstack group name.
- If you have created the technology library using the padstack group name before modification, reset the padstack group name set in the technology library using the Technology Registration Tool.  
Also, perform technology updating for PC boards and panels created using the technology library.
- If you have created a footprint dedicated to the PC board, as with the master footprint library, change the padstack group name.

## ● Matrix setting of user-defined the pin numbers in footprint.rsc

### [Function]

With Rev. 6.0, you can use the matrix with  $n \times m$  to easily define user-defined pin numbers. Accordingly, the system is modified and expanded so that the “Footprint\*TermsNameTable” format can be realized in the format below as well.

### [Operation]

```
Footprint*TermsNameTable {  
  (str1 str2 str3...)  
  (start end step)  
}
```

Condition: start <end &&step >0 or start >end &&step <0

start, end, step should be integer.

str1, 2, 3... should be character strings. You cannot specify a space, Kanji or Katakana in character strings or the user-defined pin number list is not generated.

```
Example) Footprint*TermsNameTable {  
  (“A” “B” “C”)  
  (1 10 2)  
}
```

The above example generates the following user-defined pin number list.

A1, A3, A5, A7, A9, B1, B3, B5, B7, B9, C1, C3, C5, C7, C9

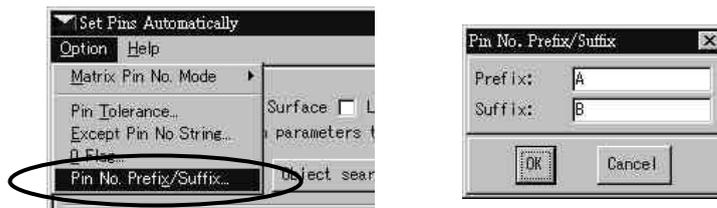
## ● Expanded automatic pin set function

### [Function]

With Rev. 6.0, you can specify a prefix or suffix for the pin numbers allocated by the automatic pin set function.

For specification, start the Pin No. Prefix/Suffix dialog box in the Set Pins Automatically dialog box.

If multiple objects are set to one pin, a warning message appears and the corresponding pin is temporarily displayed on the canvas.



### [Notes and Restrictions]

- You cannot use a 1-byte Katakana, Kanji, space or tab for the pin number prefix or suffix.

## ● Pin coordinate list input/output

The following functions are expanded for pin coordinate list output.

- [Bare chip (coordinate table loading)] function expanded
- Pin coordinate list file output function

### **[Bare chip (coordinate table loading)] function expanded**

#### **[Function]**

The following functions are expanded or changed for Rev. 6.0.

- “CSV format” file loading
  - “BGA format (CSV)” file loading
  - The “Bare chip (coordinate table loading)” label is changed to “Pin (bare chip) coordinate table loading.”
- \* This is because this function also covers items other than bare chips.

#### **[Operation]**

- (1) Specify a bare chip pad list filename in parametric registration [Pin (bare chip) coordinate table loading].
- (2) Click [Load File].

If the file is not in “bare chip pad list format” (that is, no keyword is found), the file is loaded as [CSV format]. If the file is also not in [CSV format], an error occurs.

### **Pin coordinate list file output function**

#### **[Function]**

The following functions are expanded for Rev. 6.0.

- You can output four items: X and Y-coordinates, the pin number and angle from the registered pin information to a “CSV” or “TAB” format file.
- You can output four items: X and Y-coordinates, the pin number and angle from the registered pin information to a “bare chip pad list format” file.
- You can extract four items: X and Y-coordinates, the pin number and angle from the registered pin information, add BGA parameters such as standard placement side and mounting type, and then output them to the BGA format file.

## [Operation]

- (1) Select **Utility** **Output Pin Coordinate List** to start the Wizard dialog box.
- (2) Select the items below by following the Wizard directions.
  - Output format (format and label)
  - Wire-bonding pin mode
  - Output filename
- (3) After the list is output, output results are displayed in a dialog box.



## [Notes and Restrictions]

- The unit at coordinate loading is the same as the unit selected by the active tool.
- The pin angle for coordinate loading is from  $-360.0$  to  $360.0$ . If a value exceeding this range is specified, the value is converted into an angle within the range at pin generation.
- BGA format loading loads only related information (X- and Y-coordinates, the pin number and angle).
- BGA format output outputs the following default values for items other than X and Y-coordinates, the pin number and angle.

Therefore, modify or set these parameters with the editor after output.

Net name : no setting

Net type : no setting

Pin shape : no setting

Pin dimension 1 : no setting

Pin dimension 2 : no setting

Footprint name to generate : opened footprint name

“Schematic symbol” in PCB : opened footprint name

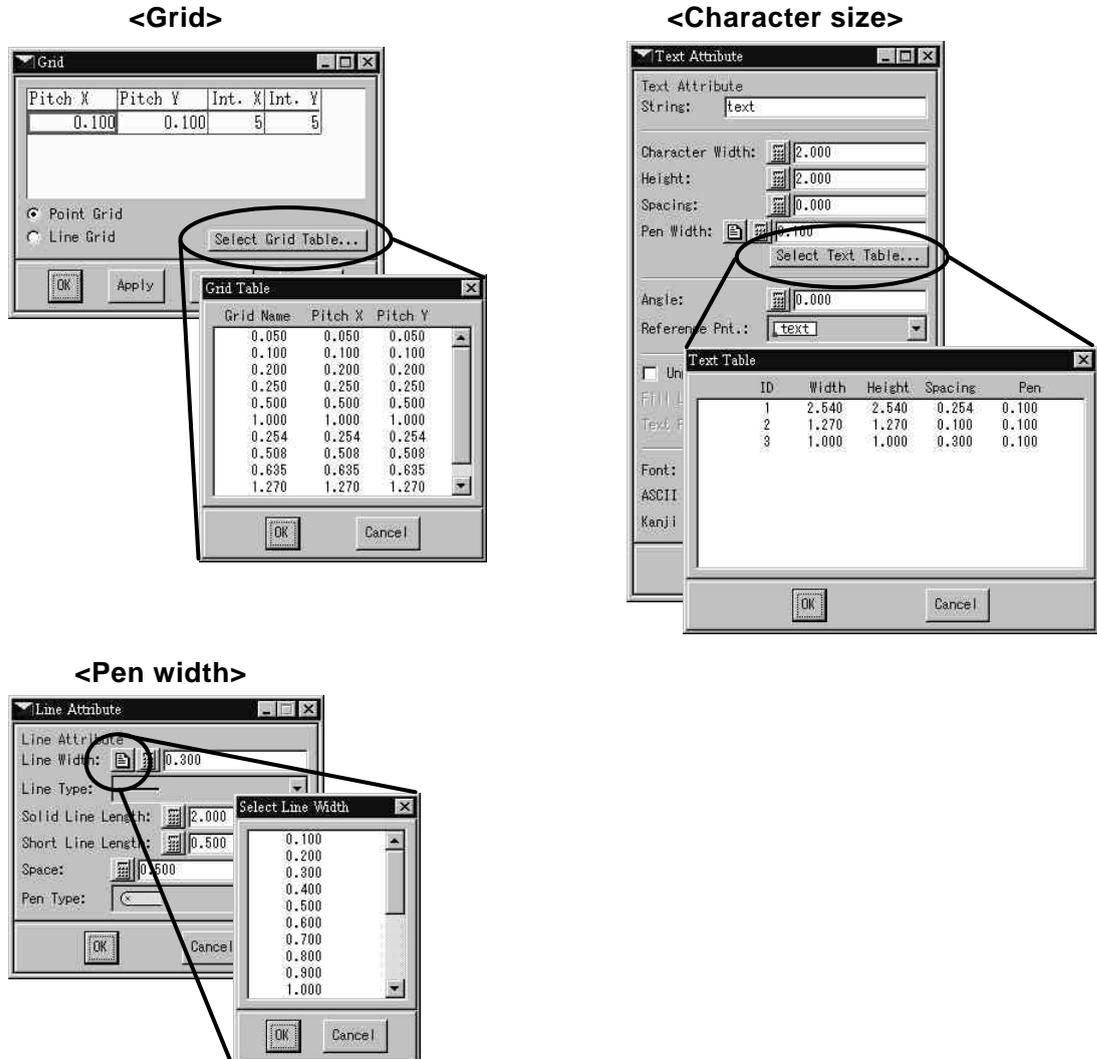
Placement side : BOTTOM

Mounting type : FC

## ● Tabulating the grids, character sizes and pen widths

### [Function]

Rev. 6.0 supports the function to tabulate the grids, character sizes and pen widths.



### [Notes and Restrictions]

- Values defined in the resource file are loaded upon tool activation. They are not reloaded while the tool is active.
- You have to define the grids, character sizes and pen widths for each tool in the resource file.

### Reference

For resource files, see “1-4 List of Changed Resource Files ?\$ZCSROOT/info/footprint.rsc, ?\$ZCSROOT/info/padstack.rsc, ?\$ZCSROOT/info/pad.rsc.”

## ● Improved function related to the point specified at figure selection

### [Function]

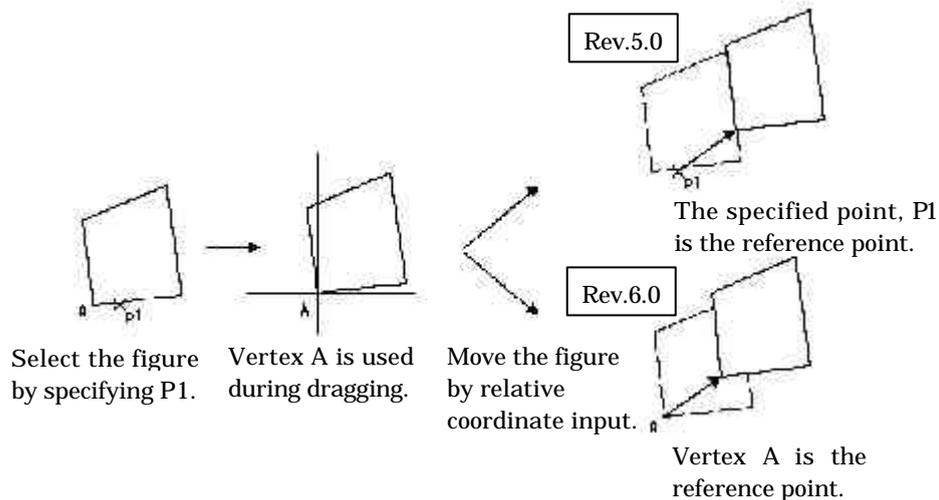
With Rev. 5.0, a specified point is the reference position when moving a figure by relative coordinate input though a vertex is dragged on the display when a drag figure is clicked with the mouse.

Rev. 6.0 has improved function so that each command moves a point specified at figure selection to figure vertex coordinates.

<Supporting commands>

- Moving by dragging
- Copying by dragging
- Adding a vertex
- Moving a vertex
- Moving a line segment
- Changing a route
- Extending and shortening a line
- Moving a wire-bonding pad
- Inputting the pin number character

During command execution, a specified point is changed to the vertex coordinates when a figure is selected, and the \* and flag marks are displayed for the vertex.



### [Notes and Restrictions]

- If [Retraction] is [OFF] when moving by dragging or copying by dragging or if [Retraction to Vertex] is [OFF] when moving the vertex or line segment, coordinates are not moved.

## ● Unified coordinate input operation

### [Function]

Coordinate input operation on the BD, BP and CDB is unified and the following points are improved.

- You can use the indicator menu at the bottom of the editor window to input coordinates on the BD and BP, in the same way as on CDB.

However, the relative point function for CDB is separated to the Assist Menu.



- You can use the Coordinate Input dialog box on CDB as on the BD and BP to specify coordinates.
- No changes are made to the current way of inputting coordinates on the BD and BP, so you can continue to use this.
- The display menus of the Coordinate Input dialog box are unified on the CDB, BD and BP. The menu has been added to **View** on the menu bar and the label is “Coordinate Input Box.”

## ● Warning message display at padstack saving

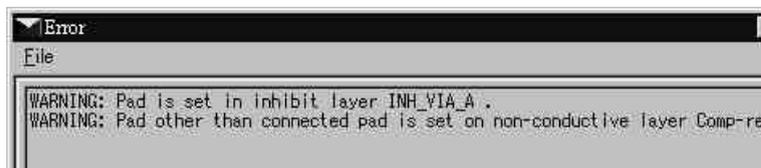
### [Function]

During padstack registration, you can

- set a pad on a keep-out layer
- set a pad with land status other than connected land (non-connected, thermal or clearance) on a non-conductive layer.

However, note that such settings are not referred to on the BD.

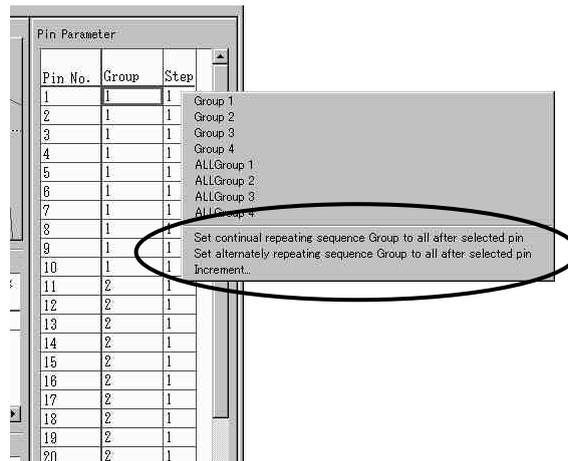
If such a pad is set, Rev. 6.0 displays a warning message when data is saved with the Padstack Registration Tool.



## ● Wire-bonding pad automatic generation pin parameter table [optional]

The following three functions are added for pin parameter table group setting for the wire-bonding pad automatic generation function to increase group setting efficiency.

- [Set continual repeating sequence Group to all after selected pin] function
- [Set alternately repeating sequence Group to all after selected pin] function
- [Increment...] setting



### **[Set continual repeating sequence Group to all after selected pin] function** **[Function]**

Start the group number set in the selected group cell and increase the following pin group numbers by a value in [Increment...].

#### **[Operation]**

- (1) Click the [group] cell in the Pin Parameter table.
- (2) Open the pop-up menu by right-clicking.
- (3) Select [Set continual repeating sequence Group to all after selected pin].

### **[Set alternately repeating sequence Group to all after selected pin] function** **[Function]**

Start the group number set in the selected group cell and alternatively increase the following pin group numbers by a value in [Increment...].

#### **[Operation]**

- (1) Click the [group] cell in the pin parameter table.
- (2) Open the pop-up menu by right-clicking.
- (3) Select [Set alternately repeating sequence Group to all after selected pin].

## **[Increment...] setting**

### **[Function]**

Specify an increment for [Set continual repeating sequence Group to all after selected pin] and [Set alternately repeating sequence Group to all after selected pin].

### **[Operation]**

- (1) Click the [group] cell in the pin parameter table.
- (2) Open the pop-up menu by right-clicking.
- (3) Select [Increment...].
- (4) Set a value in the displayed dialog box.

### **[Notes and Restrictions]**

- The default is 1.

The specification range is from 1 to (the number of groups -1).

If another value is specified, the following error message appears, directing the user to reset the increment.

(Example) when the number of groups is 4



# 2-9 LCDB-Related Tool



The following functions are added and expanded for the LCDB-related tools.

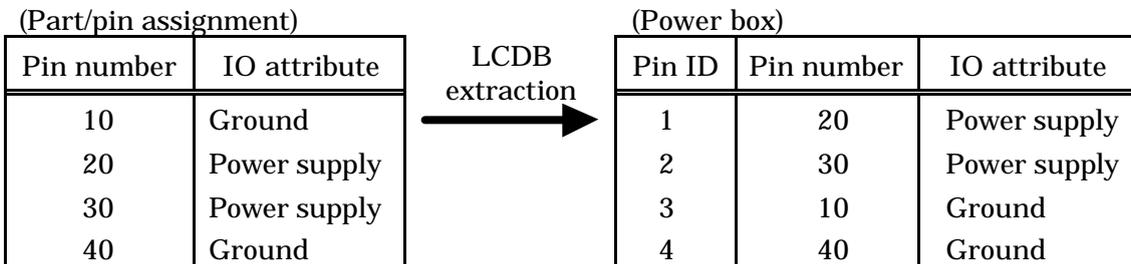
- Correspondence between power box pins and symbol pin IDs
- Deleted component support
- Changed GUI

## ● Correspondence between power box pins and symbol pin IDs

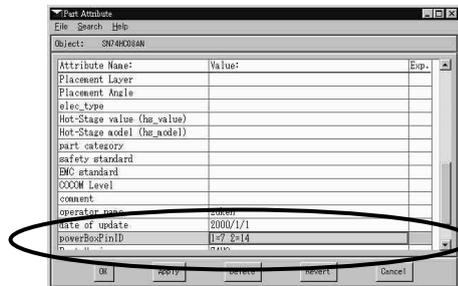
### [Function]

The Rev. 5.0 part library did not have room to store symbol pin IDs for the power box. As a result, on LCDB extraction, No.1 and subsequent numbers were set as symbol pin IDs for the power box in order from “the smallest power pin number the smallest ground pin number” as shown below.

For example, if you were using only the SD with LCDB registered with the LCDB editor and started using the BD, you would have to transfer data using the LCDB to CDF conversion program. Because the symbol pin IDs set with the LCDB editor were not necessarily the same as the IDs set on LCDB extraction on this transfer, LCDB extraction, the symbol pin IDs were changed if LCDB is re-extracted.



The Rev. 6.0 part library is equipped with an attribute to store symbol pin IDs for the power box. The IDs are stored when the LCDB to CDF conversion program is executed and referred to on LCDB extraction to maintain consistency.



### <cdb.rsc>

Item	Keyword	Value
Stores the symbol ID for the power box	powerBoxPinID	Symbol ID = pin number

## [Operation]

To start the LCDB to CDF Conversion Program (lcdb2cdf), enter the following.

```
lcdb2cdf.sh -p: outputPowerBoxPinID [Value] Required parameter
```

\* On the Windows-version, use `lcdb2cdf.exe` for activation.

## Optional parameter

```
-p: outputPowerBoxPinID [value]
```

Select one of the following for [value].

Value	Process
true	Outputs the user attributes.
false	Does not output the user attributes.

If this option is omitted, the user attributes are not output.

## [Notes and Restrictions]

- If a power box pin ID existed due to LCDB extraction processing in Rev. 5.0 explained in the previous page on [LCDB to CDF conversion program] execution, User-defined Attribute “pin ID = pin number” was not output.

## Reference

This Reference Manual on New Software Functions covers only optional parameters added to Rev. 6.0.

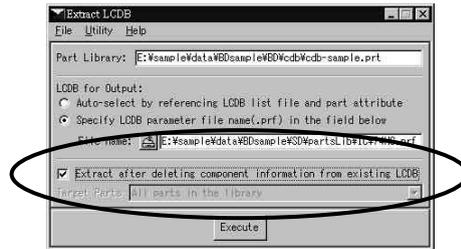
For details on `lcdb2cdf`, see the User's Guide.

## ● Deleted component support

### [Function]

If the output destination LCDB has component information deleted from the part library to be extracted, extraction is performed leaving the information as is in Rev. 5.0.

Rev. 6.0 has an added mode to delete all information in the output destination LCDB before extraction of component information so that component information in the part library and LCDB is made the same after LCDB extraction.



### <cdbabst.rsc>

Item	Keyword	Value
Specifies deletion of component information in the LCDB	CdbAbst*ReplaceLcdb	“true”: Deletes “false”: Does not delete

[When specifying a parameter to start the batch program, lcdbabst.sh]

**lcdbabst.sh -p:replaceLcdb [Value] Required parameter**

\* On the Windows-version, use lcdbabst.exe for activation.

### [Notes and Restrictions]

- If the delete mode is specified, all part information is extracted even if “CdbAbst\*ForceMode false” or the batch program starting parameter “-p:force false” is set.
- When a component not in CDB exists in LCDB, such a component is deleted from LCDB when LCDB extraction is executed in the delete mode.

### Reference

This Reference Manual on New Software Functions covers only optional parameters added to Rev. 6.0.

For details on lcdbabst, see the User’s Guide.

## ● Changed GUI

### [Function]

GUI functions for the LCDB Extraction Tool are changed in line with added functions.

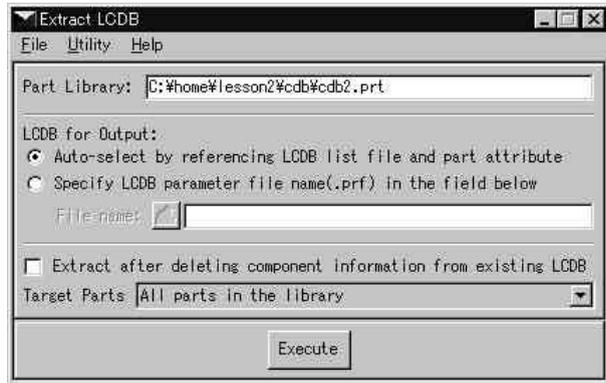
Rev.5.0



OR



Rev.6.0



## 2-10 Library Searcher/Viewer



The following functions are added for the Library Searcher/viewer.

- Template Definition Tool
- Template reloading function
- Pin number display position specification
- Expanded automatic dimension line display function
- Batch file output with the post program
- Print Property dialog box
- Changed and added keywords for the library searcher

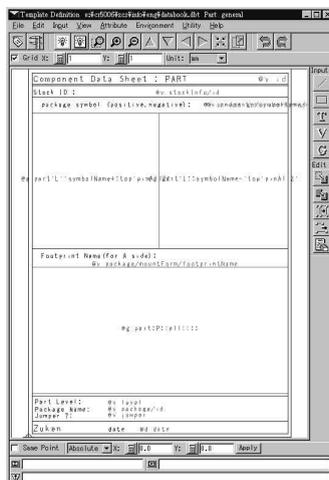
### ● Template Definition Tool

#### [Function]

To change or add the library viewer template (screen layout used when displaying component data) in Rev. 5.0, you had to edit the template definition file (databook.dbt) with a text editor.

Rev. 6.0 features a Template Definition Tool that allows editing of the template on the screen. Using this tool, you do not have to consider complicated writing formats and can visually handle data to be displayed on the library viewer. The viewer displays the saved display as soon as the template is saved, facilitating specification of displayed items.

- Creating a template
- Inputting a value
- Inputting graphics
- Changing an attribute of a displayed item



## [Operation]

- (1) Select **Utility** **Template Definition...** from the Library Viewer menu bar.
- (2) This loads the template currently used on the library viewer (selected with **Template** on the menu bar) and starts the Template Definition Tool.
- (3) Switching the viewer template switches the Template Definition Tool template.



## [Notes and Restrictions]

- The “lvt.ftp” file is created in the directory containing the databook.dbt resource file referred to by the library viewer.
- The Template Definition Tool registers template information in the databook.dbt resource file to the “lvt.ftp” file.
- Do not edit the “lvt.ftp” file using a tool other than the Template Definition Tool.

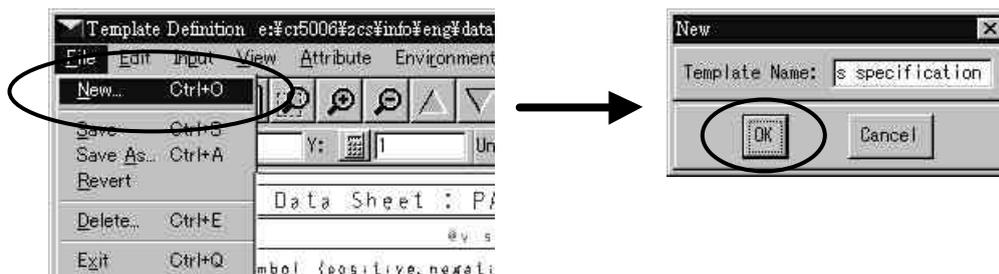
## Creating a template

### [Function]

This function creates a new template.

### [Operation]

- (1) Select **File** **New** from the Template Definition Tool menu bar.
- (2) Input a template name to create in the New dialog box.
- (3) Click **OK**.



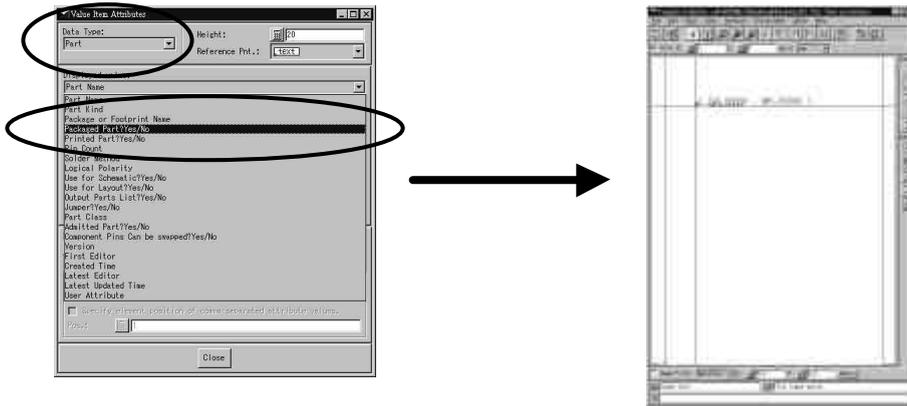
## **Inputting a value**

### **[Function]**

This function inputs information added to a part or footprint to the template.

### **[Operation]**

- (1) Select **Input** **Value** from the Template Definition Tool menu bar.
- (2) Select [Data Type] and [Displayed value] from the list in the Value Item Attributes dialog box.
- (3) Move the mouse on the canvas for the Template Definition Tool and click for display.



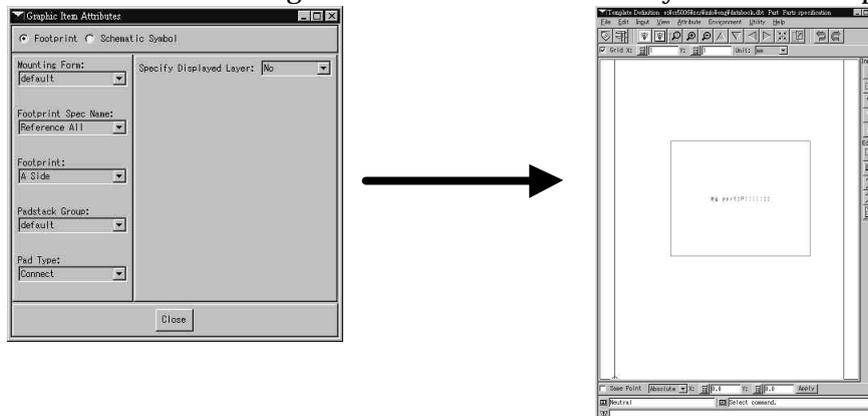
## **Inputting graphics**

### **[Function]**

This function inputs a graphic item displaying figure information (footprint or schematic symbol) into the template.

### **[Operation]**

- (1) Select **Input** **Graphics** from the Template Definition Tool menu bar.
- (2) Select data to display in the Graphic Item Attribute dialog box.
- (3) Move the mouse on the canvas for the Template Definition Tool, and then click the ends of a diagonal line in the area where you want to display it.



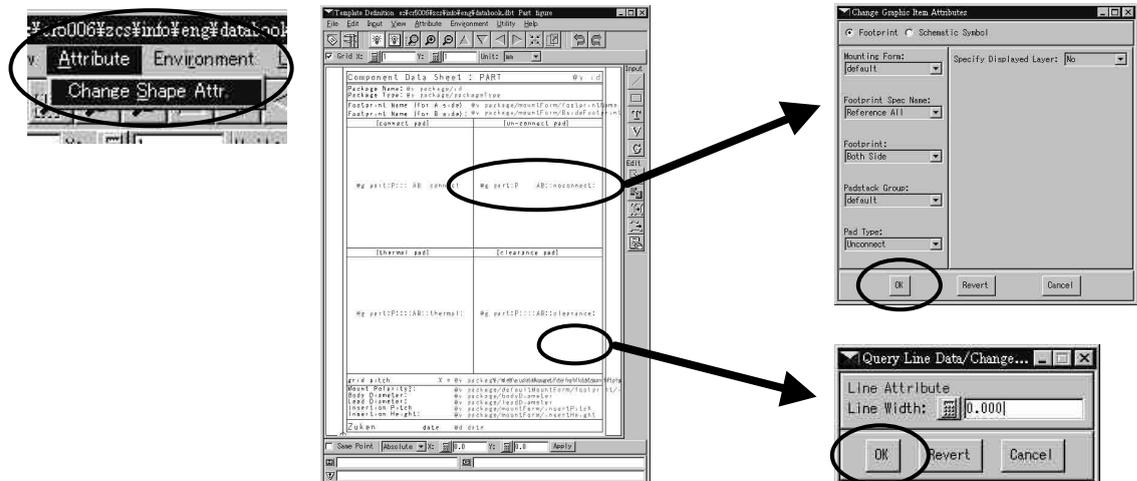
## **Changing an attribute of a displayed item**

### **[Function]**

This function refers to and changes an attribute for a displayed item.

### **[Operation]**

- (1) Select **Attribute** **Change Shape Attr** from the Template Definition Tool menu bar.
- (2) Click and select a displayed item with parameter or attribute to refer to or change on the canvas, or specify coordinates, or select by specifying an area. This starts the Change Shape Attributes dialog box.
- (3) After setting parameters in the dialog box, click **OK**.



## **● Template reloading function**

### **[Function]**

With Rev. 6.0, you can reload the databook.dbt resource file while the library viewer is active.



## **● Pin number display position specification**

### **[Function]**

With Rev. 6.0, you can specify the display position for the pin numbers.

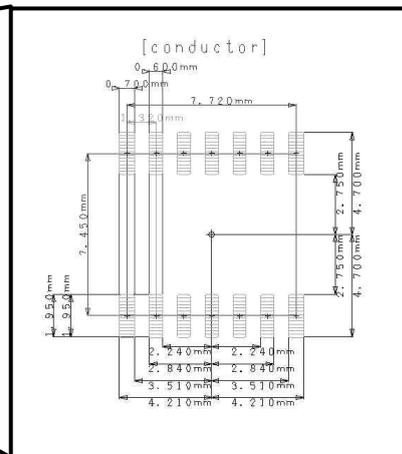
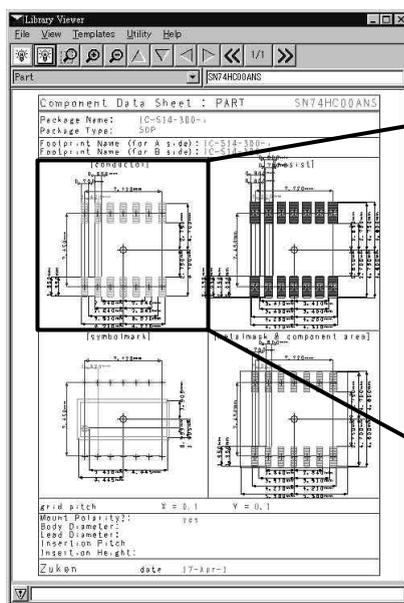


## ● Expanded automatic dimension line display function

### [Function]

The following functions are added to the Rev. 6.0 dimension line display function.

Added function	Explanation
Displays dimension lines between pins (to the origin)	1. Displays the dimension line between “the origin and pin” 2. Displays the dimension line to the nearest pin 3. Displays the dimension line to the farthest pin
Displays the pad dimension line for footprint	Specifies display of the pad (pad in padstack) width and height dimension when displaying footprints per layer
Displays the dimension line between “the origin to a vertex”	Specifies display of the distance in the X and Y directions between a vertex of an object (surface, line or component area) and the origin when displaying footprints per layer with dimensions.
Sets the dimension unit	Specifies “mm,” “inch,” “mil,” or “micron” as the dimension unit
Displays/Not displays auxiliary lines	Specifies whether to display auxiliary lines
Sets accuracy	Specifies the accuracy for distance
Sets a font for dimension line text	Specifies a font for dimension line text
Sets a character to be added to a dimension line text	Specifies display of “mm,” “inch,” “mil,” “micron” etc.
Sets a dimension line arrow shape	Specifies a dimension line arrow shape
Sets a width, height or interval for dimension line texts	Specifies a width, height or interval for dimension line character strings



The following keywords are added in line with adding new functions.

**<dimrules.dbt>**

Item	Keyword	Setting
Dimension line between [Origin and pin]	origin	set as pinPitchXY
Dimension line to the nearest pin	nearest	set as pinPitchXY
Dimension line to the farthest pin	mostdistant	set as pinPitchXY
Dimension unit	units	Specify mm, inch, mil or micron.
Dimension line auxiliary line display	assist	ON : Displays OFF : Does not display
Distance accuracy	precision	Integer between 0 and 5
Font for dimension line text	vectorFontName	Specify a font name
Character string to be displayed before the dimension line distance	preString	An arbitrary character string
Character string to be displayed after the dimension line distance	postString	An arbitrary character string (default: mm)
Dimension line arrow shape	aarrowShape	Specify None, Dot, JIS or ANSI.
Ratio of dimension line character width to rectangle width enclosing the footprint	textWidthRatio	Integer between 0 and 100
Ratio of dimension line character height to rectangle width enclosing the footprint	textheightRatio	Integer between 0 and 100
Ratio of dimension line character interval to rectangle width enclosing the footprint	textSpaceRatio	Integer between 0 and 100

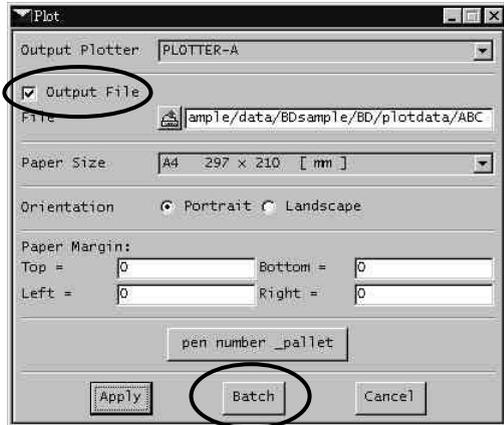
**[Notes and Restrictions]**

- The “pad dimension line display for footprint” function is valid only when footprint shapes are displayed “per layer.”
- “Display per layer” displays only dimension lines not related to the rectangle enclosing a footprint.
- Dimension between the origin and object vertexes are displayed in up to four directions: positive and negative X-directions and positive and negative Y-directions.
- When an angle other than 0° is set for padstack or pad, the dimension line is displayed if the angle is a multiple of 90°. Otherwise, the line is not displayed.

## ● Batch file output with the post program

### [Function]

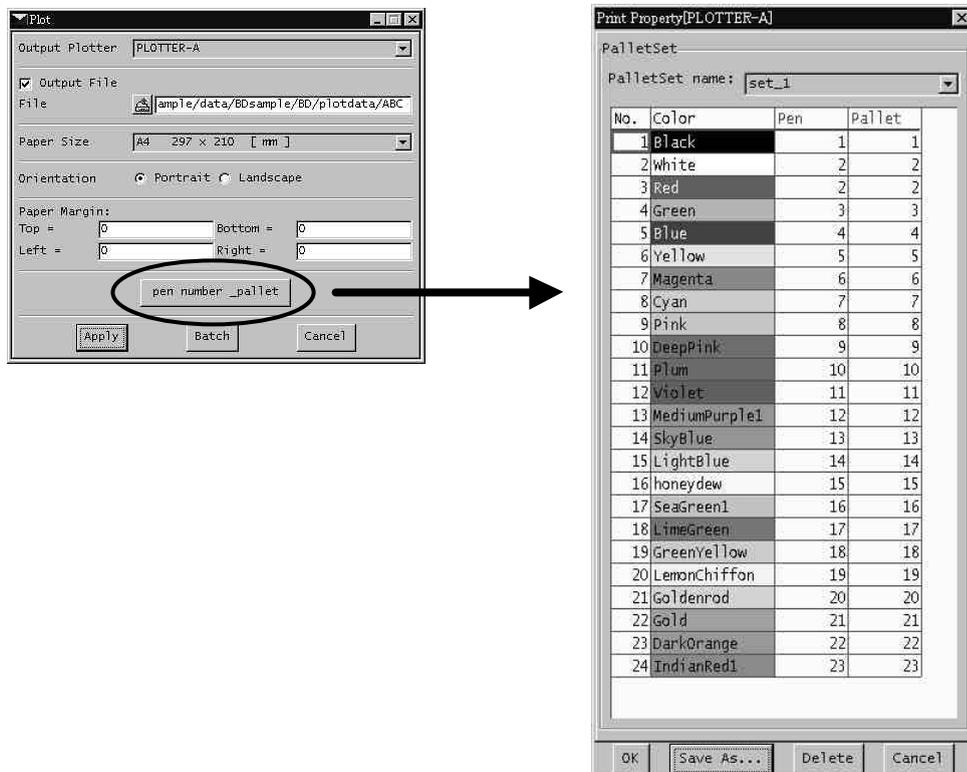
You can output files in batch using the post program. When “ABC” is specified as filename, files are output under the filename of “ABC,” “ABC2,” “ABC3”...



## ● Print Property dialog box

### [Function]

With Rev. 6.0, you can specify pen and palette numbers at printing. You can save setting and share data with the BD.



## ● Changed and added keywords for the library searcher

### [Function]

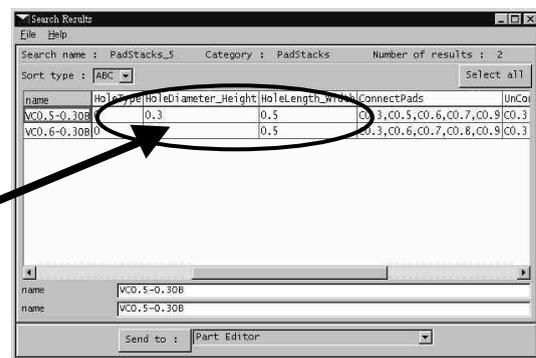
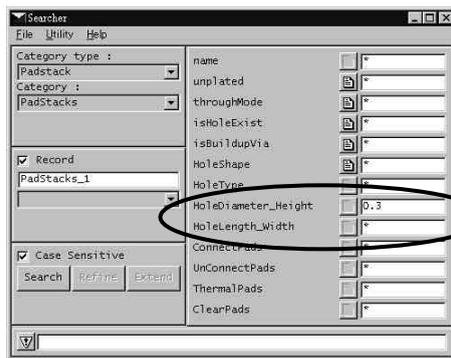
Rev. 5.0 used “holeType” as the keyword to search for a padstack hole shape.

With Rev. 6.0, “holeType” is changed to “holeShape.”

“holeType” is used to search for a hole type, as in other CR-5000 tools. The following keywords are added as well.

#### <search.rsc>

Item	Keyword	Search target
Hole shape	holeShape	[Circle], [Square] or [Oblong hole]
Hole type	holeType	Integers between 0 - 64
Diameter/height (round hole, oblong hole/square hole)	holeDiameter_Height	Real number larger than 0
Length/width (oblong hole/square hole)	holeLength_Width	Real number larger than 0



# 2-11 Expanded CDB ASCII Input/Output Function



The following functions are added or expanded for the CDB ASCII input/output program.

- Function added to output component information updated after an arbitrary date/time
- Changed processing in the part library ASCII input “modify” mode

## ● Function added to output component information updated after an arbitrary date/time

### [Function]

Rev. 6.0 has a new function to output component information updated after a specified date/time with the following ASCII output program.

#### <Supported program>

partback.sh	Part library ASCII output program
pkgback.sh	Package library ASCII output program
ftout.sh	Footprint library ASCII output program

\* On the Windows-version enter “.exe” instead of “.sh.”

You can specify the date/time in the following two ways.

- Specifies component information updated after a specified date/time  
[- p:date CC YY MM DD h mm]
- Specifies component information updated on specified days  
[- p:daybefore days]

#### -p:date CC YY MM DD hh mm

Specifies a date/time.

Symbol	Meaning
CC	the first two digits of year
YY	the third and fourth digits of year
MM	Month (01 to 12)
DD	Day (01 to 31)
hh	Hour (00 to 23)
mm	Minute (00 to 59)

\* If CC and YY are omitted, the current year is used.

\* If YY is specified but CC is omitted, the CC value would be as follow:

YY value	CC value
70 to 99	19
00 to 38	20

\* If CC, YY and MM are omitted, the current year and month are used.

\* If CC, YY, MM and DD are omitted, the current year, month and day are used.

\* hh and mm cannot be omitted.

**-p:daybefore *days***

Specifies days before the present day.

\* 0 is automatically set for “hour” and “minute.”

If “0” is specified in *days*, the present day is used.

**-p:referred [value]**

Specifies subordinate objects to output.

Select one of the following for [value].

Value	Process
all	Outputs all subordinate objects.
updated	Outputs subordinate objects updated after a specified date/time.

\* The subordinate objects for part information are pin assignment and function information.

**[Notes and Restrictions]**

- If you specify a date that does not exist, an unintended date may be used.

For example, when you specify April 32, May 2 is used.

 **Reference**

This Reference Manual on New Software Functions covers only optional parameters added to Rev. 6.0.

For details on partback, pkgback and ftout, see the User’s Guide.

**● Changed processing in the part library ASCII input “modify” mode****[Function]**

If “partconv” is executed in the “modify” mode in Rev. 5.0 when part or pin assignment information in the ASCII file defines pin-related information (interface....) or when a part or pin assignment not referred to by a part is in the part library, all pins are deleted.

With Rev. 6.0, only information in the ASCII file is changed and that not in the ASCII file is neither changed nor deleted.

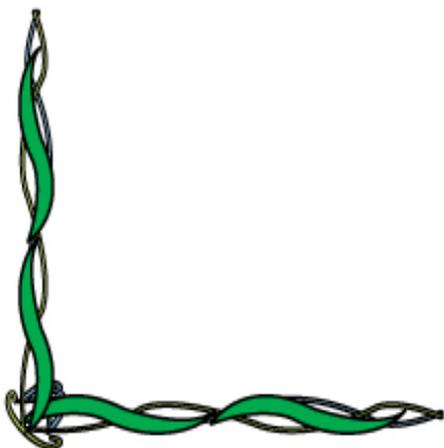
**[Notes and Restrictions]**

- If the ASCII file contains “Internal function on multiplex function specification” (func Inst.....), all reference function names, internal function pin and connection information are deleted before information in the ASCII file is set.

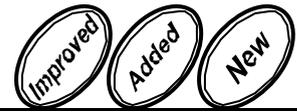


# **Chapter 3**

## **Design Preparation Tools**



# 3-1 Commonalities between Tools



The Technology Editing Tool, the Design Rule Editing Tool and the Annotation Tool support the following functions.

- Added components and net attribute support
- Deleted cancel button
- Ability to save a technology or design rule under different name

## ● Added components and net attribute support

### [Function]

Each design-preparation tool supports the net and component attributes for editing and cross-referencing added for Rev. 5.010 or newer versions. Component attributes used only in BD are supported, and not deleted during forward annotation.

Attribute	PC board generation	F/a	B/a	Design rule editing for PC board
<b>[Net rules]</b>				
Pair net name	?	?	?	?
Maximum parallel wiring length for crosstalk check	?	?	?	?
Specification prohibiting grounding	?	?	?	?
Maximum wiring capacity	?	?	?	?
Topology comment	?	?		
<b>[Electrical net rules]</b>				
Electrical net setting	?	?		
Maximum and minimum wiring lengths	?	?		?
<b>[Pin rules]</b>				
Pin series attribute for E-net evaluation	?	?		
Pin comment	?	?		
<b>[Junction rule]</b>				
Via flag	?	?		?
<b>[Pin pair group rule]</b>				
Maximum and minimum wiring lengths	?	?		?
<b>[Component rules]</b>				
Constant	?	?	?	
Component non-series attribute for electrical net evaluation	?	?		
EMC-targeted component	?	?		
Adjacent-placed group name	?	?		
Adjacent-placed component type	?	?		
Reference fixing flag	?	?	?	
Printed resistor shape, width and length		*1		
HighProbe, LowProbe or GuardPin name		*1		
<b>[Design rules]</b>				
Mesh cutout figure limit				?
Component DRC group clearance				?

? : This attribute can be set as-is.

? : This attribute is referred to.

\*1: This attribute is not referred to but not reset due to forward annotation.

For information on the tools corresponding to an attribute, see “CR-5000 User’s Guide/Correspondence table between net and component properties, and commands (tools).”

## ● Deleted cancel button

### [Function]

The [Cancel] button is deleted from the screen for design-preparation tools and third-vendor tools by using the menu bar and the [Execute] and [Cancel] buttons.

To end the action, click   or the window menu button “Exit: ×.”

## ● Ability to save a technology or design rule under different name

### [Function]

With Rev. 6.0, you can save the technology (design rule file) currently being edited with the Technology Editing Tool and the Design Rule Library Editing Tool under a different name. This function facilitates a temporary backing up of data, or the copying and reuse of data.

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## 3-2 Technology Editing Tool

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The Rev. 6.0 Technology Editing Tool supports the following function.

- Checking a prohibited character string in non-conductive layer names

### ● Checking a prohibited character string in non-conductive layer names

#### [Function]

The Rev. 5.0 Technology Editing Tool permitted registration of any names to the non-conductive layers. However, in contrast, Rev. 6.0 checks the names to avoid adding system-reserved character strings on non-conductive layer registration. This prohibits using the same non-conductive layer names as the character strings (layer name) automatically allocated by the system, and prevents malfunctioning.

The following character strings cannot be registered as non-conductive layer names. (not case sensitive).

- “ALL”
- “BASEPOINT”
- “BOARD”
- “BOARDASSY”
- “BOARDSHAPE”
- “HOLE”
- “LAYOUT”
- “PADSTACK”
- “PLACEAREA”
- “WIR”
- “WIR-ALL”
- “WIR”+number
- “WIR”+number+ arbitrary character string

If you try to add a non-conductive layer using a prohibited character string, the following error message appears.



#### [Notes and Restrictions]

- The error message does not appear when you open a technology to which a non-conductive layer using a prohibited character string is registered.

## 3-3 Design Rule Editing Tool



The following functions are added or improved for the Design Rule Editing Tool.

- Setting new rules
- Component clearance
- Improved Design Rule Selector dialog box
- Support when default padstack is not set
- Improved padstack setting (qualified padstack setting)
- Overlap check on group registration (net group setting)
- Function to classify net rules for EMC advisor
- Creating wiring width stacks by using characteristic impedance
- Expanded functions of copy rules (loading part of rule)
- Improved function to load the entire library
- Reference open function for the Design Rule Library Editing Tool

### ● Setting new rules

The following rules are added for Rev. 6.0.

- Net rule attribute
- Mesh cutout figure limit
- Maximum and minimum wiring lengths for electrical net
- Improved junction name display
- Maximum and minimum wiring lengths for the pin pair group rule

### **Net rule attribute**

#### **[Function]**

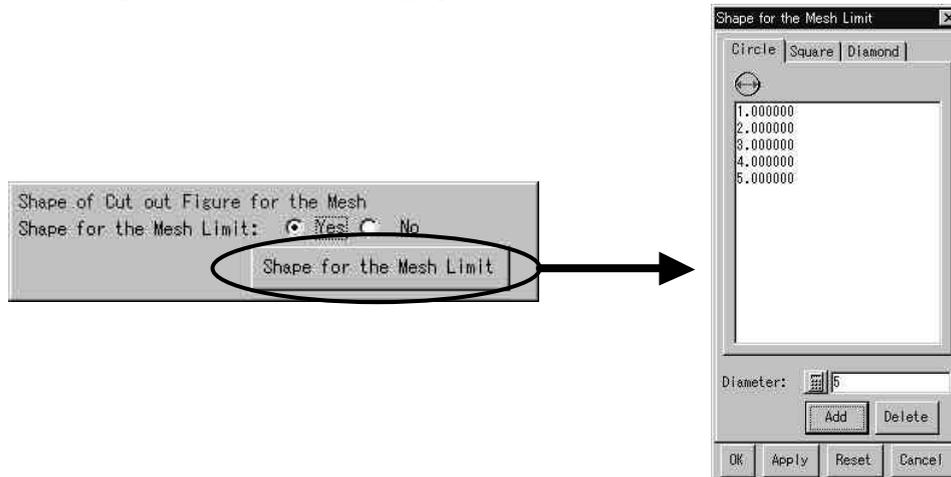
Rev. 6.0 has the following new net attributes for the EMC advisor added as net rules.

Net attribute	Explanation
Pair net name	Specified to net for pair wiring such as differential signal
Maximum parallel wiring length for crosstalk check	An attribute specified to the passive net of crosstalk. The net wiring outputting crosstalk cannot be parallel to passive net wiring longer than the maximum parallel wiring length.
Specification prohibiting grounding	An attribute specified so that a signal on the analog circuit can keep high characteristic impedance, and capacity connection with the ground may be avoided.
Maximum wiring capacity	After the total output pin drive-capacity and load pin-capacity is determined at the time of circuit design, the difference between them is specified as the maximum wiring capacity (pF).

## **Mesh cutout figure limit**

### **[Function]**

You can set Yes or No for “Shape for the Mesh Limit” and the “mesh cutout figure limit combination” attribute with “Change the Screen to Edit: board specification.” This enables the setting of a limit on combinations of cutout figures and diameters according to the manufacturing specifications.



### **Reference**

For information on meshing surfaces, see “4-7 Editing Surface ? Improved mesh function (putting and editing mesh).”

## **Maximum and minimum wiring lengths for electrical net**

### **[Function]**

Rev. 6.0 supports electrical nets, enabling the setting of maximum and minimum wiring lengths, electrical net attributes set on the schematic and also editing of net attributes.

Net Name	E-Net Max Wir. Length	E-Net Min Wir. Length	Desig Rule Stack
enetgrp-1	20.00000	10.00000	
enetgrp-2	20.00000	10.00000	
enetgrp-3	10.00000	5.000000	
enetgrp-5	100.0000	30.00000	
+12V	---	---	
-12V	---	---	
4FSC	---	---	

### **[Notes and Restrictions]**

- You cannot create an electrical net, or add or delete a consistent net with the Design Rule Editor.
- If a net name not on the PC board is set to the electrical net, the net will not be displayed in the electrical net list.

### **Reference**

For information on the electrical net, see “4-19 Electrical Net Operation.”

## Improved junction name display

### [Function]

With Rev. 5.0, junction names displayed as a pin pair rule were long and difficult to see. Rev. 6.0, however, allocates new junction names according to the following rules.

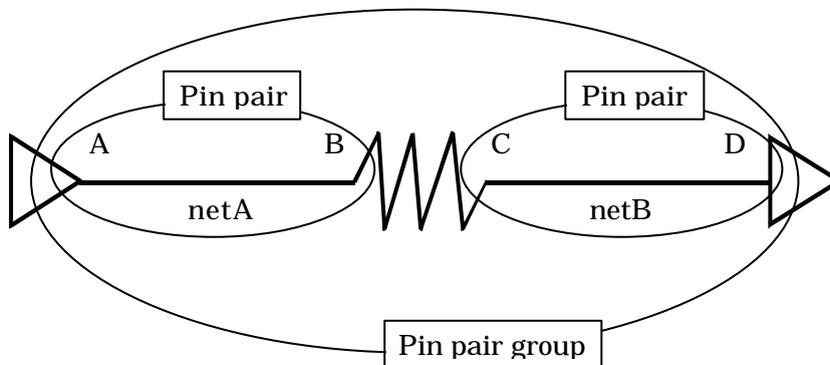
- “Junk\_” + number
- “JunkVia\_” + number

Rev.5.0		Rev.0.6	
Net Name	Pin Pair	Net Name	Pin Pair
SG00398	c26p1_c31p1 - c26p2_c16p	CSYNC#	junc_14 - R31(2)
SG00398	c2p2_c32p2_c18p1_c17p1_c	CSYNC#	junc_14 - IC1(1)
SG00398	c2p2_c32p2_c18p1_c17p1_c	CSYNC#	junc_14 - IC1(10)
SG003123	c2p1_c31p1 - c2p2_c16p1	SCLK	juncVia_1 - IC12(2)
SG003123	c2p2_c32p2_c18p1_c17p1_c	SCLK	juncVia_2 - IC3(9)
SG003123	c2p2_c32p2_c18p1_c17p1_c	SCLK	juncVia_3 - IC7(9)
SG003123	c2p2_c32p2_c18p1_c17p1_c	SCLK	juncVia_4 - IC2(12)

## Maximum and minimum wiring lengths for the pin pair group rule

### [Function]

With Rev. 6.0, you can now set the maximum and minimum wiring lengths for a pin pair group. Area DRC for the maximum and minimum wiring length covers these items.



## ● Component clearance

### [Function]

Rev. 6.0 has a new dialog box to set Component DRC group clearance for the Design Rule Edit Tool, as the Component DRC function is expanded for the Floor Plan and Placement/Wiring Tools.

Component clearance setting is referred to by the component overlapping (DRC group) of Component DRC for the Floor Plan and Placement/Wiring Tools.

- Setting a component placement side
- Setting a component type
- Setting the component alignment direction
- Setting a clearance

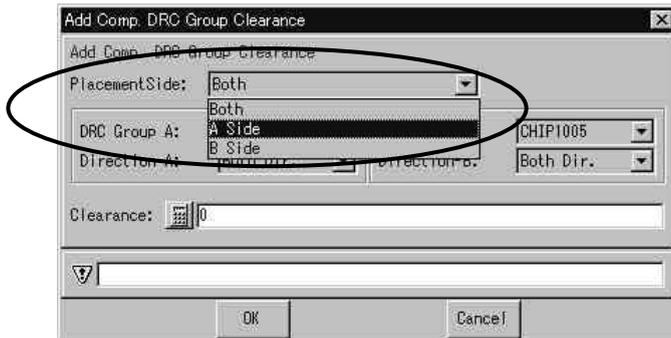
## **Setting a component placement side**

### **[Function]**

With Rev. 6.0, you can set different component clearances per component placement side. In other words, you can set different clearances on A and B sides.

### **[Operation]**

Select [Both], [A Side] or [B Side] for [Placement side] in the Add Comp. DRC Group Clearance dialog box.



### **[Notes and Restrictions]**

- When [A Side] or [B Side] is set, components on the side not set are not covered by Component DRC group check.

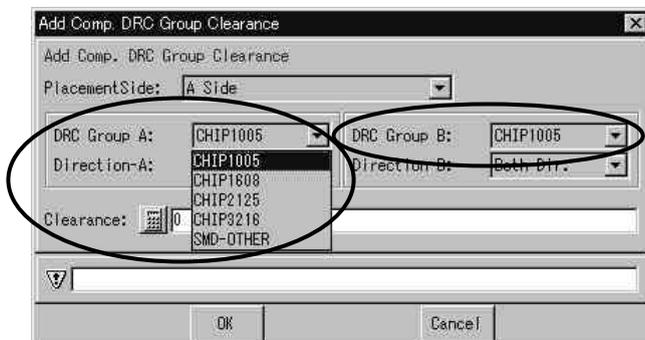
## **Setting a component type**

### **[Function]**

This function sets Component DRC groups that represent component types.

### **[Operation]**

Select a DRC group for [DRC group A] and [DRC group B] in the Add Comp. DRC Group Clearance dialog box.



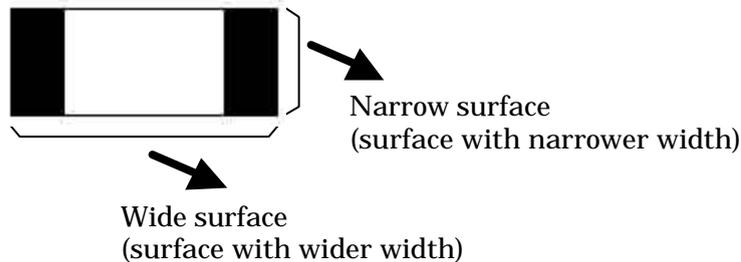
### **[Notes and Restrictions]**

- You must pre-set Component DRC groups to the package.

## Setting the component alignment direction

### [Function]

This function sets checking for Component DRC groups on either the wide surface or the narrow surface. When [All] is set, both the wide and narrow surfaces are checked.



### [Operation]

Select [Both Dir.] [wide] or [narrow] for [Direction-A] and [Direction-B] in the Add Comp. DRC Group Clearance dialog box.



## Setting a clearance

### [Function]

This function sets clearances for the component placement sides, Component DRC groups and directions.

### [Operation]

Input a clearance in the [Clearance] field in the Add Comp. DRC Group Clearance dialog box.



## ● Improved Design Rule Selector dialog box

The following points are improved for the Rev. 6.0 Design Rule Selector dialog box.

- Improved function to filter by “the number of layers”
- Design rule open attribute display
- Changing display of the dialog box without “design rule relation” definition

### **Improved function to filter by “the number of layers”**

#### **[Function]**

In Rev. 5.0, filtering by “the number of layers” was the first item in classifying design rules. Rev. 6.0, on the other hand, separates this from design rule classification and enables filtering of displayed design rule names by the number of layers at any phase.

### **Design rule open attribute display**

#### **[Function]**

The Rev. 5.0 Design Rule Selector dialog box did not list design rule files that could not be opened for “writing” because they were “Read Only” or of an older database. Rev. 6.0 displays all design rules in the design rule library by adding [X] or [RO] annotations.

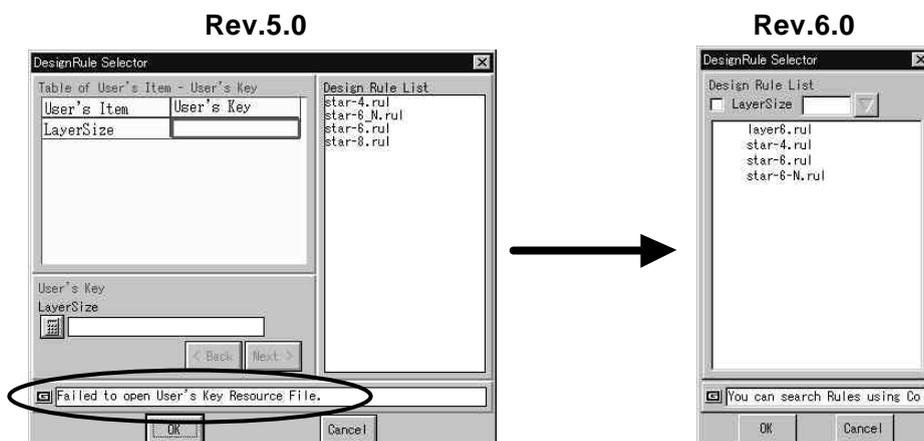
#### Reference

For information on [X] and [RO] annotations, see “3-3 Design Rule Editing Tool ? Reference open function for the Design Rule Library Editing Tool.”

### **Changing display of the dialog box without “design rule relation” definition**

#### **[Function]**

With Rev. 6.0, if a library does not contain “design rule relation” definition, the Design Rule Selector dialog box displays only the design rule name list.



## ● Support when default padstack is not set

### [Function]

With Rev. 5.0, if a single-sided wiring board did not use a wiring via, the default padstack was set as dummy and a via-inhibited figure was input on the PC board. In contrast, Rev. 6.0 allows PC board design, even if the default padstack is not set.

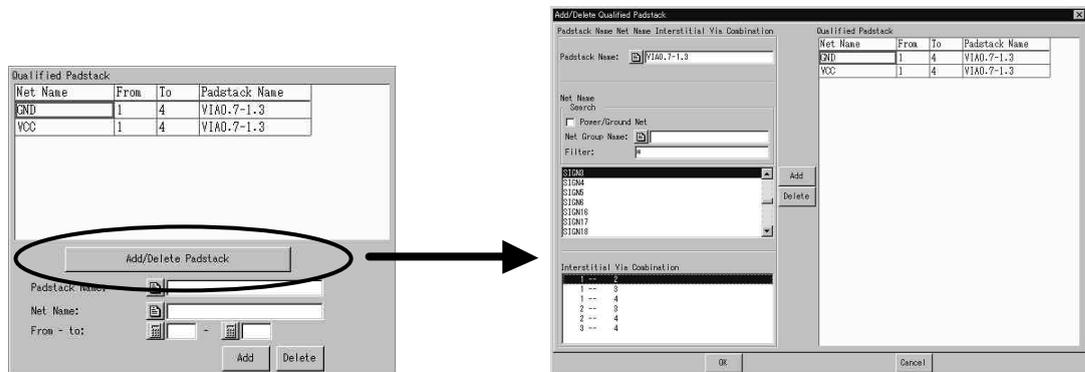
### [Notes and Restrictions]

- If a default padstack or qualified padstack is not set, you can input a wiring via on the PC board by using the copy command or the reuse command.
- There is no function to check a default padstack or a padstack not in a qualified padstack already used as a wiring via on the PC board.

## ● Improved padstack setting (qualified padstack setting)

### [Function]

Functions are added to the Rev. 6.0 “Add/Delete Qualified Padstack” dialog box, enhancing the function to edit qualified padstacks. This reduces editing work, for example, by enabling the simultaneous addition or deletion of multiple qualified padstacks.



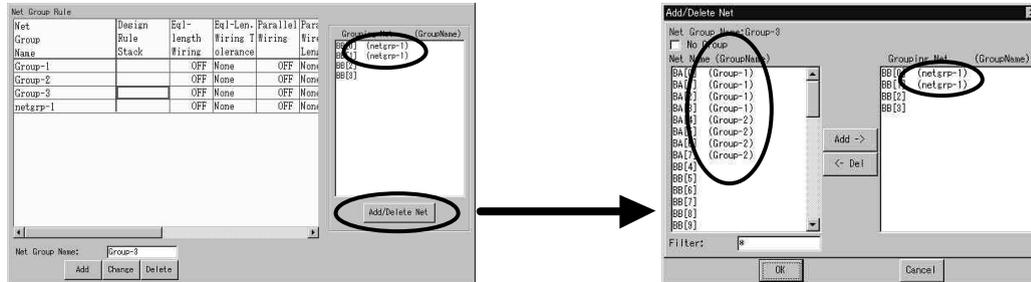
### [Notes and Restrictions]

- If a default padstack or qualified padstack is not set, you can input a Wiring Via on the PC board by using the copy command or the reuse command.
- There is no function to check a default padstack or padstack not in a qualified padstack already used as a wiring via on the PC board.

## ● Overlap check on group registration (net group setting)

### [Function]

Rev. 6.0 displays corresponding net group names next to the grouping net list displayed at net group registration and the net names in the Add/Delete Qualified Padstack dialog box. This enables you to check if a net overlaps another net group.



## ● Function to classify net rules for EMC advisor

### [Function]

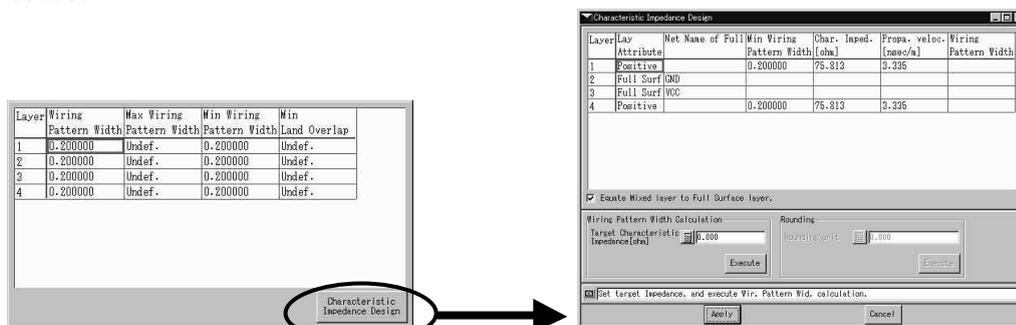
Rev. 6.0 has a new classification function for the EMC advisor to the net rule editing attribute classification items. This enables a narrowing down of the net rules used by the EMC advisor function, and their display, making setting more efficient.



## ● Creating wiring width stacks by using characteristic impedance

### [Function]

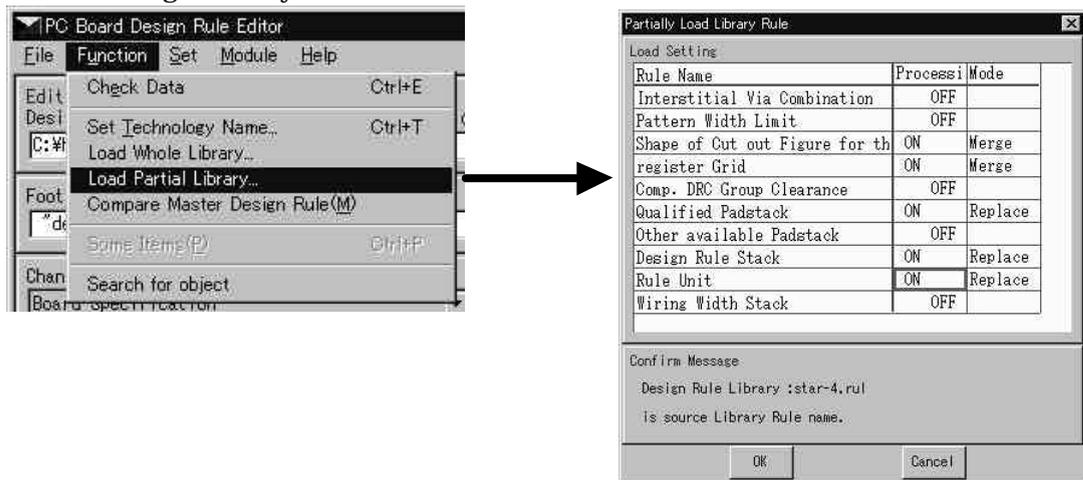
Rev. 6.0 has a new dialog box function to support the creating of wiring width stacks by using characteristic impedance. This enables determination of a wiring width with characteristic impedance when you are designing a PC board that requires consideration of transmission path characteristics such as a high-speed digital PC board.



## ● Expanded functions of copy rules (loading part of rule)

### [Function]

Rev. 6.0 can load part of the library design rules (RUL). This enables the loading of rules that require extensive input work (e.g. rules in the table format) from the existing library during design rule editing. By reusing these rules, you can save work and time when inputting rules. You can select the merge or replace the mode when loading a library.



### [Notes and Restrictions]

- If the number of conductive layers between the library design rule and PC board design rule are different, you cannot load the following rules.
  - Specifications on layer combinations
  - Qualified padstack
  - Design rule stack
  - Wiring width stack
- “Specifications on layer combinations” and “pattern width limit” are loaded regardless of the settings for “Limits on Interstitial Vias (Yes or No)” and “Pattern width limit (Yes or No).”
- When the “design rule stack” is loaded, “unit names” not registered in advance are not loaded.
- Once part of a library is loaded, you cannot undo the operation by clicking [Cancel] or [Reset].

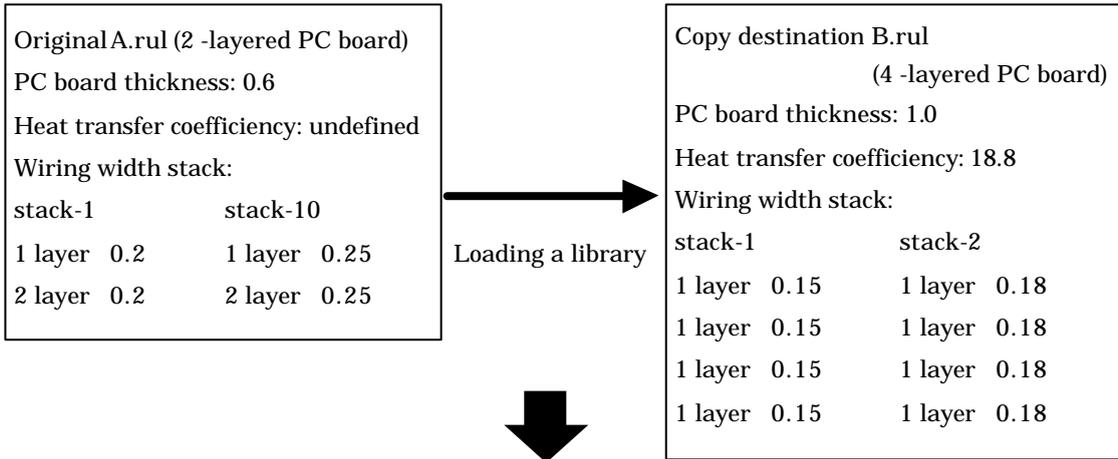
## ● Improved function to load the entire library

### [Function]

Rev. 5.010 did not reset attributes that were not set in the original library but were set in the copy destination and left as they were when the entire library was loaded.

In contrast, Revs. 5.020 and 6.0 have an improved function to clear all editable attributes in the design rule library and replace them with the attributes in the specified design rule.

### <Difference between Rev. 5.010 and Rev. 5.020 and 6.0>



	Rev. 5.010	Rev. 5.020 and 6.0
No. of layers	2-layered PC board	2-layered PC board
PC board thickness	0.6	0.6
Heat transfer coefficient	18.8	undefined
Wiring width stack:	stack-1    stack-2    stack-10	stack- 1    stack- 10
	Layer 1 0.2    undefined    Layer 1 0.25	Layer 1 0.2    Layer 1 0.25
	Layer 2 0.2    undefined    Layer 2 0.25	Layer 2 0.2    Layer 2 0.25

### [Notes and Restrictions]

- The following information related to net names become undefined.
  - Full surface net name
  - Specified qualified padstack name
- If a rule refers to the design rule stack and wiring width stack, the stack name becomes undefined.
  - Net rule (design rule stack, wiring width stack and shield wiring width stack)
  - Pin pair rule (wiring width stack)
  - Net group rule (design rule stack)
  - Net-group group rule (design rule stack)
- Once you have executed the function to load the entire library, you cannot stop operation by clicking [Cancel] or [Reset].

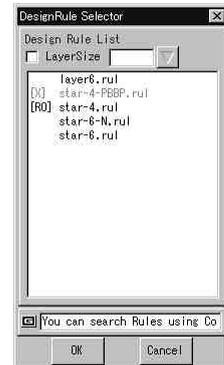
## ● Reference open function for the Design Rule Library Editing Tool

### [Function]

With Rev. 6.0, you can open or check design rules using the Design Rule Library Editing Tool even if you do not have the Write permissions for the design rule file in the directory specified as the design rule library.

At the same time, the design rule utility can differentiate three types of design rule files for display.

Symbol	Design rule open attribute	Selection
(no symbol)	Can be opened and rewritten	Possible
[RO]	Can be opened for reference	Possible
[X]	Cannot be opened	Impossible



### [Notes and Restrictions]

- For “open for reference”, the database is displayed by temporarily copying the design rule file to Environmental Variable TMPDIR (UNIX-version) or TMP (Windows-version) and opening the temporary file. Therefore, you need the Write permissions for the TMP directory.
- If you specified the “Read Only” attribute to the folder specified as “design rule library” on the Windows-version, it is assumed that you do not have the Write permissions for the folder and, therefore, you cannot open design rules in the library for purposes other than reference.

# 3-4 Board Generation Tool



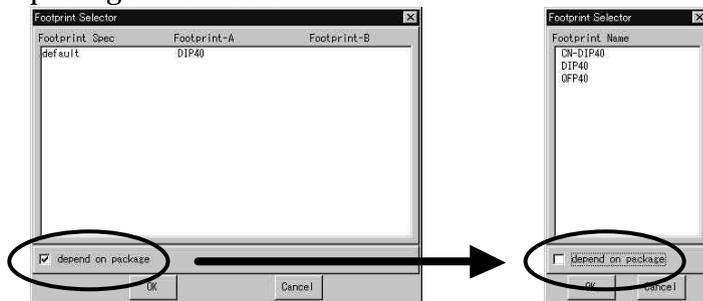
The following functions have been added for the temporary footprint assignment function for the Board Generation Tool.

- Assignment function for package-independent footprints
- Function added to check unadmitted parts

## ● Assignment function for package-independent footprints

### [Function]

By using the Footprint Selector started from the Footprint Assignment dialog box for the Board Generation Tool, you can assign footprints other than those registered in package information.



### [Notes and Restrictions]

- If the “depend on package” check box is cleared, the dedicated footprint and footprint libraries are searched for footprints with the same number of pins as the part referred to by the component and those with the same pin number and corresponding footprint names are listed.

## ● Function added to check unadmitted parts

### [Function]

Rev. 5.0 continued with the process regardless of whether an unadmitted part was being used. Rev. 6.0 has an improved function to display a warning message with unadmitted part reference when an unadmitted part is used. The same warning message appears on forward annotation.



## 3-5 Annotation Tool



The following functions are added or improved for the Forward Annotation Tool.

- Added function for pin and gate swapping list output
- Modification of the change confirmation list display file
- Added History GUI function
- Change in active design change UI
- Expanded temporary footprint assignment function
- Preventing edited in-component figures from disappearing
- Forward annotation function for wiring width
- Expanded jumper operation function
- Changed land status normalization function
- Added message output function
- Supporting PC board net color design change

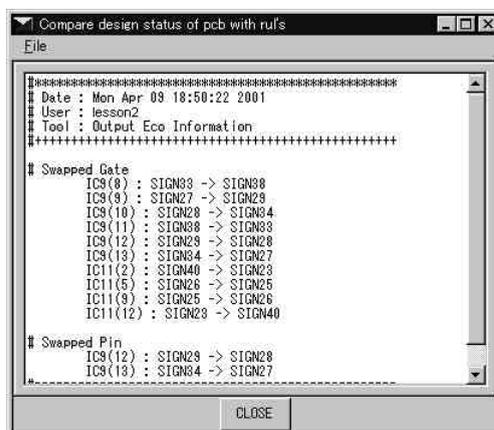
### ● Added function for pin and gate swapping list output

#### [Function]

Rev. 5.0 listed pin swapping and gate swapping in the “changed net assignment” item when selecting **Confirm** **Output diff &PCB and RUL** from the menu bar for the Forward or Back Annotation Tool started from the File Manager.

For Rev. 6.0, items, “pin swapping” and “gate swapping” are added to classify pin swapping and gate swapping.

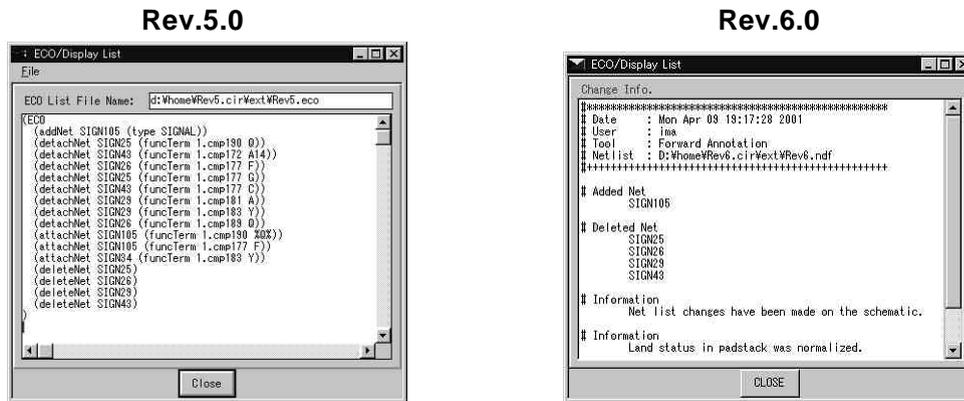
#### Rev.6.0



## ● Modification of the change confirmation list display file

### [Function]

In Rev 5.0, when the Forward or Back Annotation Tool started from the File Manager was activated, selecting **Confirm** **Confirm Change** from the menu bar displayed the ECO file. In Rev. 6.0, the same operation displays the COH file.

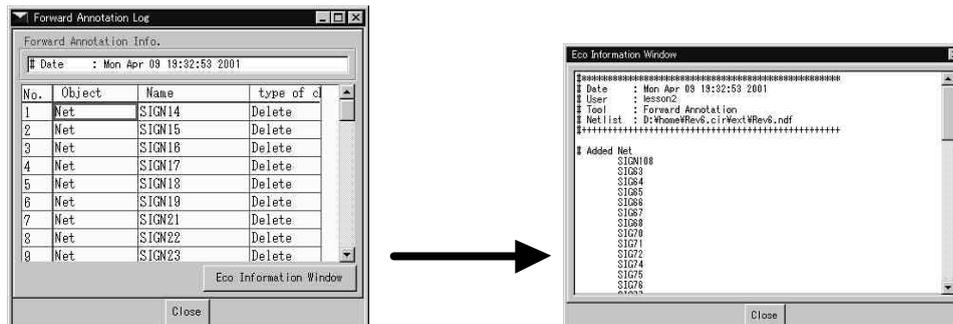


## ● Added History GUI function

### [Function]

Rev. 6.0 displays design changes in the Forward Annotation Log dialog box added to Rev. 6.0, as well as the screen display used in Rev. 5.0, when forward annotation is executed with the Placement/Wiring Tool.

Selecting **Utility** **Forward Annotation** **Forward Annotation Log** from the menu bar redisplay the changes.



## ● Change in active design change UI

### [Function]

This was started by selecting **Utility** **Forward Annotation** from the menu bar in Rev. 5.0 during forward annotation executed with the Placement/Wiring Tool.

In Rev. 6.0, this is started by selecting **Utility** **Forward Annotation** **Set Net List**.

## ● Expanded temporary footprint assignment function

The following functions are added for temporary footprint assignment.

- Improved processing when using a component not in the library
- Assignment function for package-independent footprints

### **Improved processing when using a component not in the library**

#### **[Function]**

If you use a footprint with a different relationship from that specified in CDB on the PC board during temporary footprint operation and the following values have been set in board.rsc, the Footprint Assignment dialog box shown below appears. This enables checking of a footprint temporarily used on the PC board and changing it to a formal footprint.

<board.rsc>

Item	Keyword	Value
Displays the component using a package-independent footprint	displayIncompleteComp	“On”: Displays such components “Off”: Does not display such components



#### **[Notes and Restrictions]**

- The existing edited in-component figures are deleted when package-independent footprints are changed.
- Information changed using the Footprint Assignment dialog box is saved in “PC board name.ft9.” You can delete “xx.ft9” when forward annotation is complete.

### **Assignment function for package-independent footprints**

#### **[Function]**

As with the Board Generation Tool, you can assign footprints other than those registered in package information by using the Footprint Selector started from the Footprint Assignment dialog box.

#### **Reference**

For more information on this function, see “3-4 Board Generation Tool ? Assignment function for package-independent footprints.”

## ● Preventing edited in-component figures from disappearing

### [Function]

On Rev. 5.0, if you have performed land-cut or silk shape editing for a component on the PC board, and then changed the part name of the symbol corresponding to the component on the schematic, the execution of the Forward Annotation Tool changes the component part name on the PC board and resets the edited figures in the component. Rev. 6.0 has been improved not to reset edited in-component figures when the following design changes are made.

- Component type changed
- Component part name changed
- CDB part name changed (the number of pins and the pin numbers are not changed)

Change	Rev. 5.005/Rev. 5.010		Rev. 5.020/Rev. 6.0	
	Component symbol	Other figures	Component symbol	Other figures
Component type changed	Deleted	Deleted	Not deleted	Not deleted
Component part name changed	Not deleted ██████████ ██████████ ██████████	Deleted	Not deleted ██████████ ██████████ ██████████	Not deleted ██████████ ██████████ Not deleted ██████████ ██████████ Deleted
CDB part changed (the number of pins and the pin numbers are not changed.)	Not deleted	Deleted	Not deleted	Not deleted
CDB part changed (the number of pins and the pin numbers are changed.)	Deleted	Deleted	Deleted	Deleted
Component reference changed	Not deleted ██████████ ██████████ ██████████ ██████████	Not deleted	Not deleted ██████████ ██████████ ██████████ ██████████	Not deleted

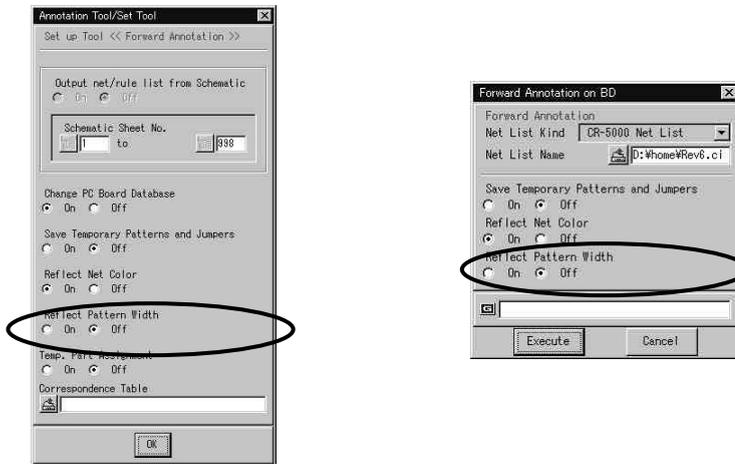
### [Notes and Restrictions]

- When a footprint related to a part is changed during “component part name change,” figures other than component symbols are reset.
- When a pin number or the number of pins is changed during “CDB part change,” all Edited in-component figures, including component symbols, are reset.

## ● Forward annotation function for wiring width

### [Function]

With Rev. 6.0, you can perform forward annotation for wiring width.



<FA Tool>

<Active FA Tool>

### <board.rsc>

Item	Keyword	Value
Reflects the wiring width	fwrAnnoUpdatePatternWidth	“On”: Reflects the wiring width “Off”: Does not reflect the wiring width

## ● Expanded jumper operation function

### [Function]

With Rev. 5.0, if you had generated a jumper component registered under the following rules on the PC board, active forward annotation deleted the jumper component.

With Rev. 6.0, this jumper can be retained during active forward annotation.

### <Rule>

- Target component of back annotation : Yes
- Part type : Jumper component

Set the following in board.rsc.

### <board.rsc>

Item	Keyword	Value
Specifies to ignore jumpers during active forward annotation.	dynEcoIgnoreJumper	“On”: Retains jumpers “Off”: Does not retain jumpers

## ● Changed land status normalization function

The following functions are added for “land status normalization” of padstacks on forward annotation.

- Changed land status normalization processing
- Added land status history file (LOH) function

### **Changed land status normalization processing**

#### **[Function]**

Board Designer has a build-in function to automatically change land status in order to optimize it for the current padstack and conductor connection.

Rev. 5.0 performed “land status normalization” for all padstacks on forward annotation regardless of changes in the net list.

Rev. 6.0 determines whether to perform “land status normalization” depending on the design change type as shown below.

Design change requiring normalization	Design change not requiring normalization
<ul style="list-style-type: none"><li>• Change in the part library</li><li>• Change in the part referred to by a component</li><li>• Deletion of a component</li><li>• Deletion of a net</li><li>• Addition of a net</li><li>• Change in the symbol assignment</li><li>• Change of the component type</li><li>• Change in the package component referred to by a component</li></ul>	<ul style="list-style-type: none"><li>• Addition of a component</li><li>• Change in the stock code referred to by a component</li><li>• Change in a reference</li><li>• Change of net name, net type or net color</li><li>• Addition of symbol</li><li>• Change in the part referred to by a symbol</li><li>• Change of the lock mode for a symbol</li><li>• Change of a component ID</li><li>• Addition and deletion of a component group</li><li>• Deletion of an unnecessary part, pin assignment and function from the PC board</li></ul>

#### **[Notes and Restrictions]**

- Land status normalization is performed for all padstacks except “Wiring Via and pin without allocated net.”

## **Added land status history file (LOH) function**

### **[Function]**

Rev. 6.0 has a new function that outputs a warning message and the land status history file (LOH) when the land status is changed.

```
#####  
# Date      : Mon May 28 18:47:04 2001  
# User      : lesson2  
# Tool      : Forward Annotation  
#####  
1:[111.765,45.727] SR1.8-0.5 (connect->nocconnect)  
1:[113.035,45.727] SR1.8-0.5 (connect->nocconnect)  
1:[38.000,66.775] SR1.25-1.1 (connect->nocconnect)  
1:[39.000,68.000] VCO.7-0.3-0.4 (connect->nocconnect)
```

<Land status history file>



<Warning message>

## **● Added message output function**

### **[Function]**

With Rev. 5.0, if you had not performed back annotation for net attributes set on the PC board, forward annotation initialized the set attributes.

Rev. 6.0 has a new function to output a warning message if the design rule database (RUL) contains set net attributes but the attributes are not set in the design rule list (RUF) to be reflected with forward annotation.

### **[Notes and Restrictions]**

- The warning message does not appear when forward annotation is performed with CCF or ECF, because the Design Rule list is not referred to.
- When the net is deleted, the warning message does not appear for the attributes of the deleted net.

## ● Supporting PC board net color design change

### [Function]

Rev. 6.0 enables the display of tone and hatching in addition to net colors in the net display on the PC board. Therefore, if the PC board net display color on the schematic is reflected with forward annotation after the tone or hatching display is set on the PC board, the set tone or hatching display is reset and only a specific color is reflected.

PC board net color on the schematic	Undefined																			
	Blue																			
	Red																			
PC board net color on the PC board <b>(before FA)</b>	Color	Undefined																		
		Blue																		
	Tone																			
	Hatching																			
Forward annotation executed																				
PC board net color on the PC board <b>(after FA)</b>	Color	Undefined																		
		Blue																		
		Red																		
	Tone																			
Hatching																				

( indicates the "net colour on the PC board" changed to depending on the "Net color on the Schematic" after forward annotation.)

### [Notes and Restrictions]

- The design changes in the above table presumes that forward annotation is performed with the Design File Manager; after the net color is set on the PC board, back annotation resets design rules.

### Reference

For information on hatching per net and displaying tone, see "4-14 Set Net Display Color Dialog Box ? Display mode setting."

# 3-6 Technology Update Tool



The following functions are added or improved for the Technology Update Tool.

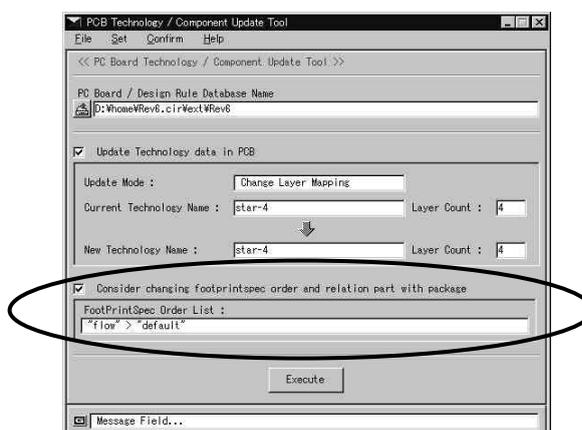
- Integration with the Footprint Specification Name Batch Reflection Program (ftsback)
- Specification to save in-component edited shapes
- Improved internal processing for Full Surface net names
- Switching the footprint update mode
- Function to save component symbols
- Improved land status normalization processing
- Changed GUI
- Function to check footprint history
- Integration with the Design Rule Editor for the PC board

## ● Integration with the Footprint Specification Name Batch Reflection Program (ftsback)

### [Function]

With Rev. 5.0, you have to use the Footprint Specification Name Batch Reflection Program (ftsback) in addition to the Technology Update Tool to reflect changes to the PC board even when changing technologies along with changed footprint specifications. Rev. 6.0 built the Footprint Specification Name Batch Reflection Program (ftsback) into the Technology Update Tool so that you can execute it as needed.

	Rev.5.0	Rev.6.0
Changes due to changed relationship between part and package in the CDB	Cannot be reflected	Can be reflected
Changes due to changed relationship between package and footprint in the CDB	Cannot be reflected	Can be reflected
Changes due to modified footprint specification name priority	Cannot be reflected	Can be reflected

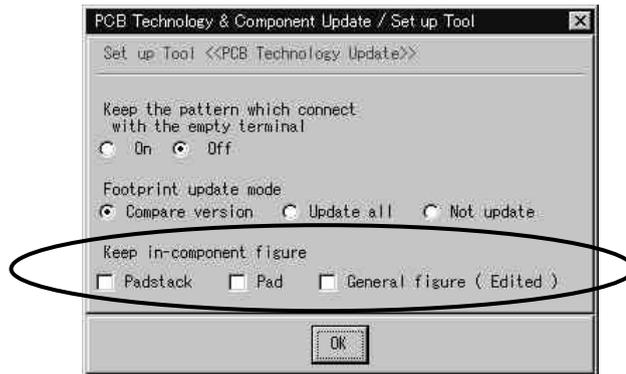


## ● Specification to save in-component edited shapes

### [Function]

With Rev. 5.0, if you reloaded updated footprint shapes from CDB, for components with updated footprints, the edited in-component shapes on the PC board are all reset and changed to shapes registered in the footprint library.

With Rev. 6.0, you can save these edited in-component shapes by specifying the [Tool set] parameter.



## ● Improved internal processing for Full Surface net names

### [Function]

With Rev. 5.0, the net names for Full Surface layers are reset upon technology updating.

With Rev. 6.0, the wiring layer attribute for the technology is changed as follows.

#### <Change in the wiring layer attribute>

- Other than Full Surface to Full Surface
- Full Surface to other than Full Surface
- Maintaining Full Surface
- Maintaining other than Full Surface

### Reference

For details on this process, see “Board Layout System/Board Designer User’s Guide, Vol.1, Design Preparation /5.2.3.5 Full Surface net name.”

## ● Switching the footprint update mode

### [Function]

With Rev. 5.0, PC board footprint update during technology update was performed by comparing the version numbers of the objects on the PC board to those with the same name in the footprint library.

With Rev. 6.0, the [Tool set] parameter has the following three modes so that you can select a process.

Existing footprint update mode	Processing
Compare version	Updates by comparing version numbers as on Rev. 5.0.
Update all	Updates all footprints, padstacks and pads on the PC board from CDB.
Not update	Does not update from CDB (* See [Notes and Restrictions].)

### [Notes and Restrictions]

- In the “Not update” mode, components are not updated from the CDB. However, to maintain footprints in the PCB, layer mappings for the old and new technologies are compared by using figure information in the PCB, and while the figures are moved or copied between layers with the same mappings, figures on layers with different mappings are lost. If hole layer mapping is changed or is not set, an error occurs.

#### Reference

For details on this process, see “Board Layout System/Board Designer User’s Guide, Vol.1, Design Preparation/5.2.4 Updating the footprints in the PC board.”

## ● Function to save component symbols

### [Function]

With Rev. 5.0, component symbols added to a PC board component with the Artwork Tool were reset (deleted) if the footprint for the component was updated.

With Rev. 6.0, such component symbols are not reset and saved after updating.

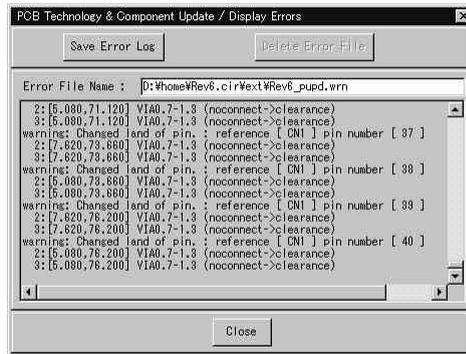
## ● Improved land status normalization processing

### [Function]

With Rev. 5.0, land status normalization was always performed for all padstacks at technology updating.

With Rev. 6.0, land status normalization is performed only for padstacks requiring the process. This enables preservation of the land status before technology updating.

When land status normalization is performed, the following warning message appears.



### Reference

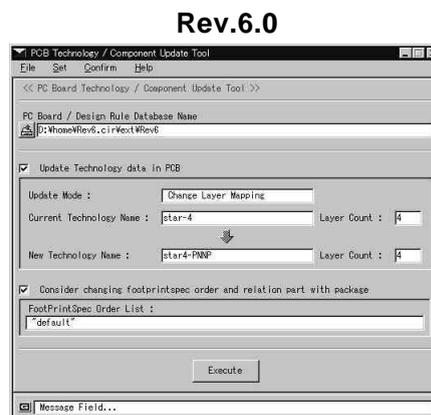
For details on this process, see “Board Layout System/Board Designer User’s Guide, Vol.1, Design Preparation/5.2.3.6 Padstack layer land status (Land status normalization).”

## ● Changed GUI

### [Function]

The Technology Update Tool dialog box has been changed as shown below in line with integration of the Footprint Specification Name Batch Reflection Program.

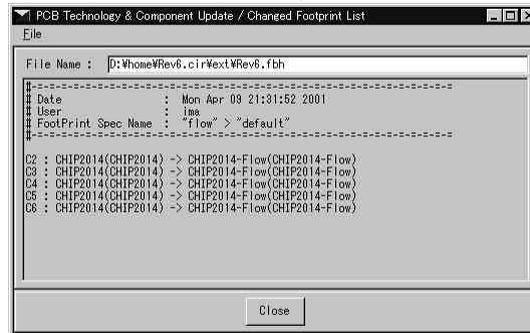
The tool name has also been changed from [PC Board Technology/Footprint Update Tool] to [PC Board Technology/Component Update Tool].



## ● Function to check footprint history

### [Function]

The footprint update list has been added. This is used to check changes in the footprint when technology updating is performed with “Consider changing footprint spec order and relation part with package” ON.



## ● Integration with the Design Rule Editor for the PC board

### [Function]

To change the technology name on the PC board in Rev. 5.0, you had to start the “Design Rule Editor for PC board” from the File Manager, change the technology name, and then start and execute the “Board Technology Tool.”

With Rev. 6.0, you can start the “PC Board Technology/Component Update Tool” by selecting **Module** **Update PC Board Database...** on the “Design Rule Editor for PC board.” If technology names for the PCB database (PCB) and design rule database (RUL) are different when the “Design Rule Editor for PC board” is ended, the following dialog box appears, enabling activation of the “PC Board Technology/Component Update Tool.”



### [Notes and Restrictions]

- If you have started the “PC Board Technology/Component Update Tool” by selecting **Module** **Update PC Board Database...**, the Design Rule Editor for the PC board is shaded and unavailable.
- Due to “Integration with Design Rule Editor for PC board,” the “PC Board Technology/Component Update Tool” can only be started from the “Design Rule Editor for PC board,” which is started from the Design File Manager.

## 3-7 Other Improvements



The following functions have been added or improved for Rev 6.0.

- ECF editor (part library reference function)
- New Component Comparison Program for PCB and CDB
- New Technology List Output Program
- New Net List Output Program
- Net List Comparison Program (part name comparison mode)

### ● ECF editor (part library reference function)

#### [Function]

A function has been added to refer to the part library when adding references with the ECF editor. This enables automatic generation of the SYMBOL section after acquiring the necessary information to add the section when a component using a part with pin assignment is added (reference addition).

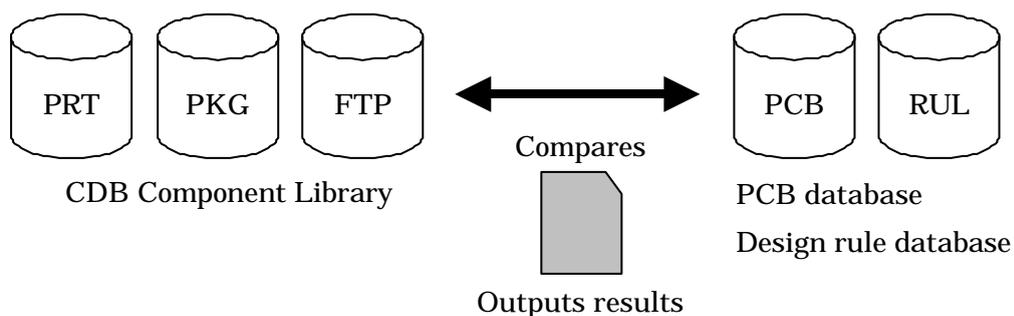
### ● New Component Comparison Program for PCB and CDB

#### [Function]

This program compares component information between the CDB and PCB databases and outputs the results.

You can check changed PC board components by executing this program before or after forward annotation or execution of the Technology Update Tool.

- Compares user versions
- Compares relations (Outputting footprints other than default)
- Compares relations (Outputting footprints inconsistent with footprint specification names)
- Compares relations (Outputting footprints inconsistent with the package library)
- Outputs edited components



## [Operation]

To start the PCB/CDB Component Comparison Program (cmpdiff), enter the following.

<code>cmpdiff.sh</code>	<b>Required parameter</b>	<b>[Optional parameter]</b>
-------------------------	---------------------------	-----------------------------

\* **On the Windows-version, use cmpdiff.exe for activation.**

### 1. Required parameter

**PC board name**

Path name without extension for the PCB and design rule files.

### 2. Optional parameter

**-l reference library name**

This is to refer to libraries other than the part library, package library and footprint library in the CR-5000 library resource file (library.rsc). Specify it with an extension.

\*If this is omitted, the part library, package library and footprint library in library.rsc are referred to.

**-m version**

This mode is specified to search the CDB for objects with the same name as the objects in the PCB database and list objects with different user versions.

\*If this is omitted, user versions are not compared.

However, if all the options beginning with “-m” including this option are omitted, user versions are compared.

**-m link, -m link1 or -m link2**

This mode is specified to check that the parts, packages and footprints referred to by components in the PCB database are assigned according to the footprint specification names and to list inconsistent ones.

link: All the footprints, other than default, cause errors.

link 1: If the footprint corresponds to the specified footprint specification name, it does not cause an error even if the footprint is not default.

link 2: If the footprint corresponds to the specified footprint specification name, it does not cause an error even if the footprint is not default.

The components using the footprint defined in the package are output to the warning section.

\* If this is omitted, relation comparison (default footprint) is not performed.

However, if all the options beginning with “-m” including this option are omitted, the process is performed.

**-m edited**

This mode is specified to check all components in the PCB database and list the components that refer to edited footprints (land-cut or silk-cut).

\*If this is omitted, the edited components are not output. However, if all the options beginning with “-m” including this option are omitted, the edited components are output.

**-o output filename for comparison results**

Output filename for comparison results.

\*If this is omitted, the results are output to the standard output.

**-V**

This outputs version information.

## ● New Technology List Output Program

### [Function]

tchlist, the program to list data in the technology library has been released. This enables output of technology information in an easy-to-recognize format.

List output examples

```

#*****
# Tool name: technology list
# Execution date/time: Sat Mar 31 11:12:13 2001
# User: user1
# File: E:\sample\data\BDsample\BD\tch\tch-sample.tch
#+*****+

* Technology name: L4-PMMP-RF
* Number of conductive layers: 4
* Padstack group name: default
* Rule area layer : Off
* Auxiliary connection information layer : Off
* Dielectric area figure layer : Off

■■■■ Conductive layer ■■■■
Conductive layer   Soldering   Layer attribute

```

## [Operation]

To start the Technology List Output Program (tchlist), enter the following.

```
tchlist.sh [Optional parameter]
```

\* **On the Windows-version, use tchlist.exe for activation.**

### Optional parameters

#### **-r reference filename**

This is used to refer to technology databases, PCB databases or panel databases other than the technology library in the CR-5000 library resource file (library.rsc). Specify it with extension.

\* If this is omitted, the technology library in library.rsc is referred to.

#### **-m list**

This lists all technology names in the specified file.

\* This option cannot be omitted. However, omission is possible if -m all or -p:name is specified.

#### **-m all**

Outputs all technology information in the specified file.

\* This option cannot be omitted. However, omission is possible if -m list or -p:name is specified.

#### **-p: name technology name**

Outputs information on a specified technology.

\* This option cannot be omitted. However, omission is possible if -m list or -m all is specified.

#### **-o output filename**

Output filename.

\* If this is omitted, information is output to the standard output.

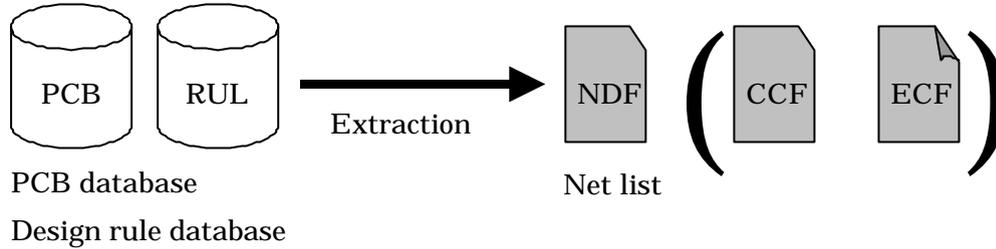
#### **-V**

Outputs version information

## ● New Net List Output Program

### [Function]

With Rev. 6.0, you can output logical net list information from the PCB database (PCB) or design rule database (RUL).



### [Operation]

To start the Net List Output Program (netout), enter the following.

```
netout.sh    Required parameter    [Optional parameter]
```

\* **On the Windows-version, use netout.exe for activation.**

#### 1. Required parameter

**PCB database name**

Path name for the PCB database (design rule database) to be extracted.

#### 2. Optional parameter

**-r input database name**

Specify this option with extension to specify a database to be input.

**-o output net list filename**

Specify this option with extension to the output net list file.

\*If this is omitted, the output filename is PCB database name.NDF.

**-m rul**

Specify this option to output the net list from the design rule database (RUL).

\* If this is omitted, the net list is output from the PCB database (PCB).

**-m CCF\_form**

Specify this option to output data in CCF format.

In the CCF mode, if the number of characters for an ID (reference, part or net) in the database character exceeds 20, the ID is shortened to the first 20 characters. Lower-case characters in ID are changed to upper-case characters.

\* If this is omitted, data is output in NDF format.

**-m ecf\_form**

Specify this option to output data in ECF format.

\*If this is omitted, data is output in NDF format.

**-m force**

Specify this option to overwrite at the time of output.

\*If this is omitted, overwriting is not possible.

**-m nochk\_len**

Valid only in the CCF output mode (-m CCF\_form).

This parameter is used to output IDs as they are to the CCF file even if characters in ID in the database are more than 20.

\*If this is omitted, the number of ID characters is limited.

**-m nochg\_id**

Valid only in the CCF output mode (-m CCF\_form).

This parameter is used to output IDs as they are to the CCF file even if some ID characters in the database are lower-case letters.

\*If this is omitted, ID lower-case characters are limited.

**-m n o\_jumper**

Valid only in the PCB mode.

This parameter is not used to output net list information on jumper components from the PCB database.

\*If this is omitted, the net list information on jumper components is output from the PCB database.

**-p: clm the number of columns**

Valid only in the CCF and ECF output mode.

This parameter is used to specify the maximum number of columns for CCF and ECF file outputting.

\* If this is omitted, 80 columns are used for output.

**-e error filename**

Output filename for error messages.

\*If this is omitted, messages are output to the standard output.

**-w warning message filename**

Output filename for warning message.

\*If this is omitted, messages are output to the standard output.

**-V**

Outputs version information.

## ● Net List Comparison Program (part name comparison mode)

### [Function]

Rev. 6.0 has a new part name comparison mode for the Net List Comparison Program (bdncmp). This enables comparison of part names used by components between the schematic net list (NDF) and pattern connection pin list (SDF).

#### **-m partname**

Compares part names.

\*If this is omitted, part names are not compared.

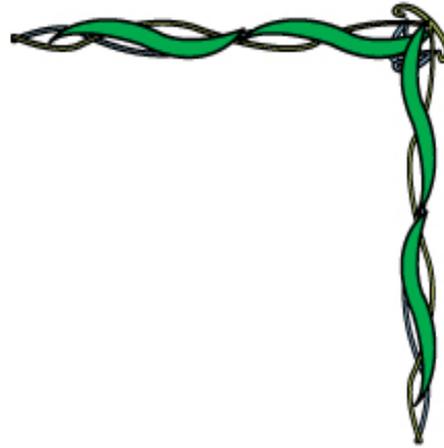
#### Output example

<<<Unmatched PartName >>>	<NDF>1	<NDF>2
R88	MCR10EZHZ103	MCR10EZHZ102
R100	MCR10EZHZ103	MCR10EZHZ102
U50	UPC324G2_A	UPC324G2_B

#### Reference

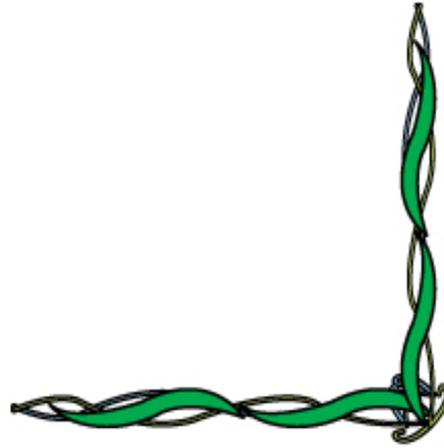
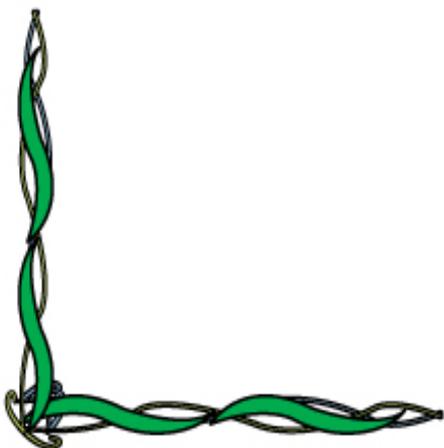
This Reference Manual on new software functions covers only optional parameters added to Rev. 6.0.

For details on bdncmp, see the User's Guide.



# Chapter 4

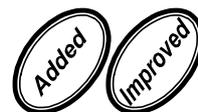
## Placement/Wiring Tool



---

# 4-1 Component Placement DRC Function

---



The following functions are added or improved for the Component DRC in the Floor Plan and Placement/Wiring Tools.

- Expanded component DRC function
- Component DRC based on Component DRC group clearance setting
- Added or improved check items
- Improved Component DRC error display

## ● Expanded component DRC function

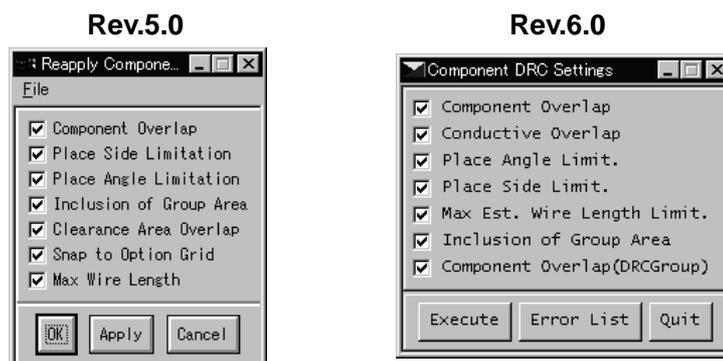
### [Function]

With Rev. 5.0, you set items to check only by batch Component DRC in the “Reapply Compone...” dialog box.

For Rev. 6.0, this dialog box’s name is changed to “Component DRC Settings” and this dialog box is referred to for the whole Component DRC.

This is referred to for the following checks.

- Online DRC (DRC directly before component placement)
- DRC re-check (DRC after the placement position is fixed)
- Batch Component DRC (Batch DRC for placed components)



You can perform the following operations in the Component DRC Settings dialog box.

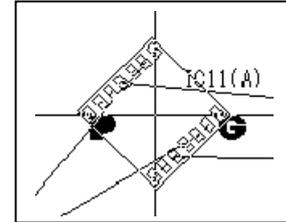
- Setting check items
- Batch Component DRC execution
- Starting the “Error List” dialog box

## [Operation] (online DRC)

- (1) Select On to **DRC** → **Online DRC** from the menu bar.
- (2) Select **DRC** → **Component DRC set...** from the menu bar.
- (3) Select the check boxes for items to check by online DRC.
- (4) Select **Edit** → **Move Component** from the menu bar to move the component.

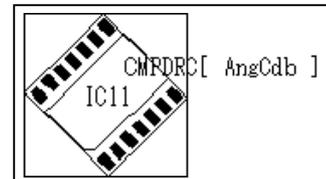
When placement is made to the move destination, online DRC prohibits placement that does not satisfy the check items.

In this case, a message such as “ Online Comp DRC Error: angle limit (CDB)” appears in the message area.



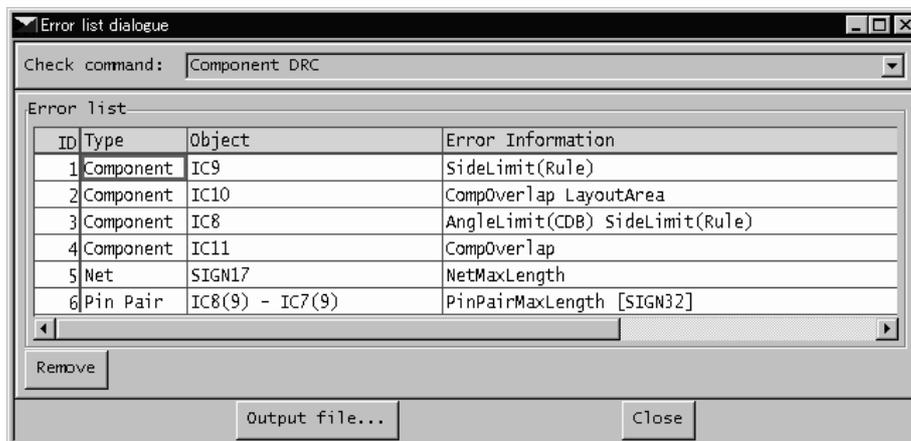
## [Operation] (Batch Component DRC)

- (1) Select **DRC** → **Component DRC set...** from the menu bar.
- (2) Select the check boxes for items to check by batch Component.
- (3) Click [Execute].



## [Operation] (Error List dialog box)

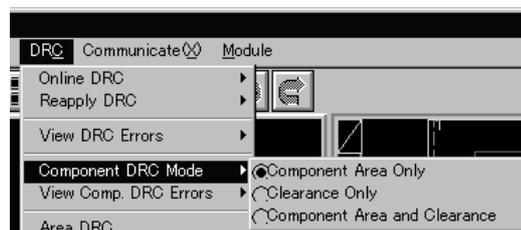
- (1) Select **DRC** → **Component DRC set...** from the menu bar.
- (2) Click [Error List].



## [Notes and Restrictions]

- As online Component DRC comes to refer to the “Component DRC Settings” dialog box, the Component DRC mode setting is not necessary.

### <Rev. 5.0 menu bar>



## ● Component DRC based on Component DRC group clearance setting

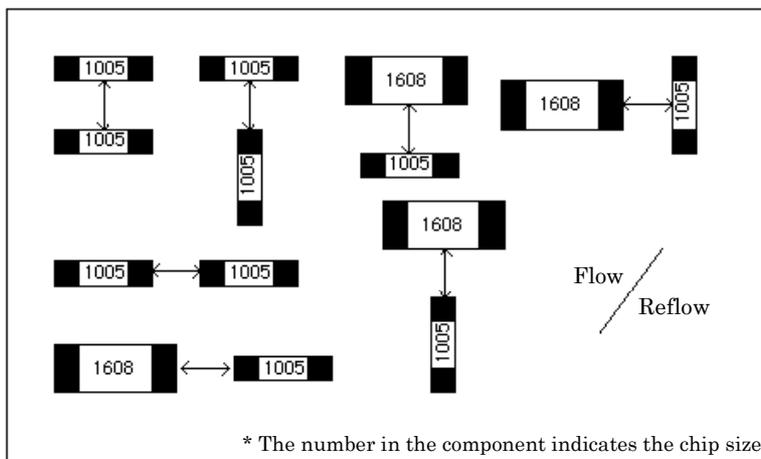
### [Function]

To support different clearances due to chip component and other soldering, with Rev. 6.0 you can set clearance between two components to actually check per

- Component placement side
- Component type
- Component alignment direction

and check them with Component DRC.

### <Cases that clearance setting is recommended>



Setting clearance according to component combination is called “Component DRC group clearance rule” (hereafter, “clearance rule”). The clearance rule consists of a rule and clearance value. You can register multiple clearance rules. When Component DRC checks clearance between two components, the clearance specified by the clearance rule with a consistent rule is employed. If there are multiple consistent rules, the largest clearance is employed.

### [Operation]

- (1) Select **DRC** → **Component DRC set...** from the menu bar.
- (2) Set **Component overlap (DRC group)** to ON in [Component DRC set].

### [Operation] (Necessary preparations)

- Before setting Component DRC group clearance, [Component DRC group] should be set to the package referred to by the component.
- To set Component DRC group clearance, use the “Component DRC group clearance set” function for the Design Rule Editor.

### Reference

To set the Component DRC group clearance, see “3-3 Design Rule Editing Tool

- Component clearance.”

## ● Added or improved check items

### [Function]

The check items related to component placement are added or improved for Rev. 6.0.

Added items

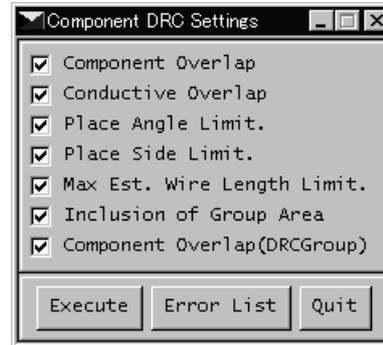
- Conductor overlap
- Component overlap (DRC group)

Improved items

- Component overlap
- Placement angle limit
- Placement side limit

Deleted items

- Expanded area overlap
- Snap to option grid



### Conductor overlap

This checks overlap with conductive figures as the “clearance” check set by selecting **DRC** → **Component DRC mode** from the menu bar on Rev. 5.0.

### [Notes and Restrictions]

- Online DRC regards a padstack in the component or component pin currently dragged as non-connected land.
- Even if the conductor overlap mode is active, the online check is not performed in the following cases:
  - Placement Keep-out and Wiring Keep-out figures in the component being dragged
  - Conductive figure (excluding component pin) to conductive figure in the component being dragged
  - Component pin to temporary conductive figure (without net) in the component being dragged
  - When a component is moved, the mode is [Push-aside Component] or [Reroute].
  - Jumper component generation and moving

### Component overlap (DRC group)

Check is performed according to Component DRC group clearance rules.

### Component overlap

The Overlap check is not performed between component and layout area if the component’s footprint attribute (Attribute name: ignoreLayoutArea, attribute value: YES/NO) is set to YES.

### Placement angle limit

Check is performed for the angle limit set in the part or footprint attribute (Attribute name: placementAngle, attribute value: angle permitted for placement) as well as the angle limit set as the conventional design rule.

### Placement side limit

Check is performed for the placement side limit set in the part or footprint attribute (Attribute name: placementLayer, attribute: A/B/Both/Neither) as well as the placement side limit set as the conventional design rule or placement limit due to correspondence between part and soldering.

When the package type is SMD, placement on the Wiring Keep-out layer and the inner-layer component placement is checked.

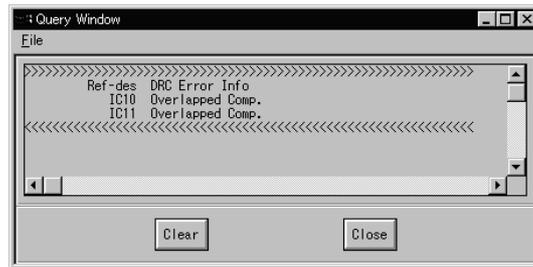
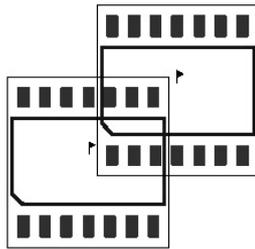
## ● Improved Component DRC error display

### [Function]

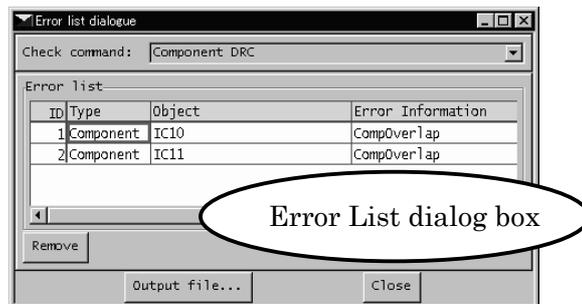
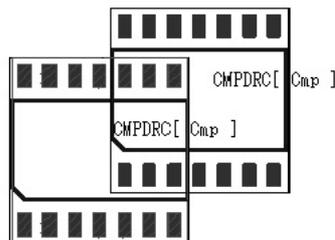
Because Rev. 5.0 only displays the flag mark to indicate Component DRC errors, it is difficult to locate an error and impossible to check the error details.

Specifications for the Component DRC have been integrated with Area DRC for Rev. 6.0, enabling display of detailed error information.

#### Rev.5.0



#### Rev.6.0



Check item	Check content/description in error list	Description on canvas	Error type
Component overlap	Component overlap	Cmp	Component
	Placement Keep-out	Plnh	
	Height limit	Hei	
	Layout area	Lay	
Component overlap (DRC group)	Component overlap (DRC group)	CmpDrcGrp	
Conductor overlap	Wiring Keep-out	Wlnh	
	Via Keep-out	Vlnh	
	Hole	Hol	
	Wiring	Wir	
Placement angle limit	Angle limit (rule)	AngRul	
	Angle limit (CDB)	AngCdb	
Placement side limit	Placement side limit (rule)	SideRul	
	Placement side limit (CDB)	SideCdb	
	Placement side limit (soldering)	SideSol	
	Placement side limit (package)	SidePkg	
	Placement side limit (conductive surface)	SideCnd	
Maximum virtual wiring length limit	Net maximum wiring length	NetMax	Net
	Net PP maximum wiring length	NetPPMax	Pin pair
	PP maximum wiring length	PPMax	
Group area enclosure	Group enclosure	InGrp	Component

### [Notes and Restrictions]

- If Component DRC error display is not activated, errors are not displayed in the error list.

# 4-2 Real Number Settable as the Component Angle

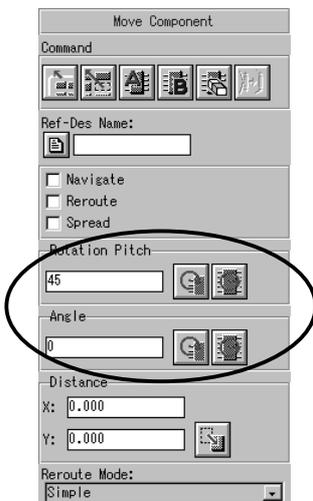


## [Function]

With Rev. 5.0, you can use only integers to specify a component placement angle.

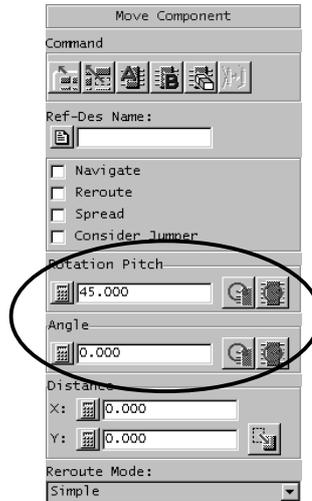
With Rev. 6.0, you can specify an angle in detail because real numbers are now settable.

### Rev. 5.0



■ ■ ■ Component ■ ■ ■ (package symbol)  
 Reference: IC1  
 Coordinates: [43.180,7.620]  
 Placement angle: 0  
 Placement side: A-side

### Rev. 6.0



■ ■ ■ Component ■ ■ ■ (package symbol)  
 Reference: IC1  
 Coordinates: [43.180,7.620]  
 Placement angle: 0.000  
 Placement side: A-side

## [Notes and Restrictions]

- The component angle should be a real number between 0 and 360 (excluding 360), with up to three digits valid below the decimal point. The fourth and following digits below the decimal point are ignored.
- The following tool and operation do not support the real number yet.

Tools (operation) not supporting real numbers	Reason
Component placement angle limit in the design rule database (RUL)	The angle is specified in 45° units.
Quick thermal	The angle is maintained in 45° units.
BD to ICX conversion, XTK interface and Apsim interface	The tools support only integers.

## 4-3 Component Operations



The following functions are added for component operation.

- Improved component move command
- Improved component change and generation commands
- Improved CDB component copy function
- Added or improved CDB component update function
- Pad editing (supporting the same net surface loading)
- Reference change lock flag
- Function to delete components not used from the PC board

### ● Improved component move command

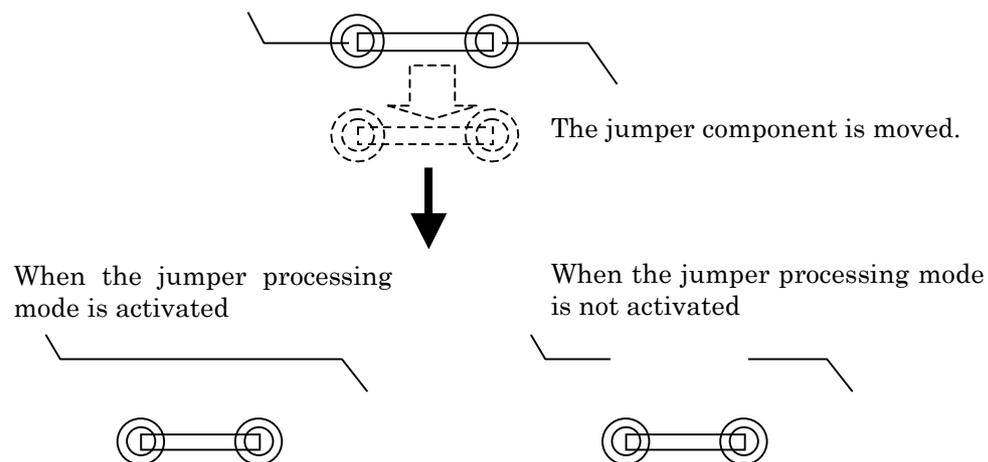
Operations are improved as follows for wiring-related commands.

- Specifying the jumper processing mode (ON or OFF)
- Three-point rotation of component

### Specifying the jumper processing mode (ON or OFF)

#### [Function]

If the jumper processing mode is activated, in Rev. 6.0, wirings connected to component pins are re-connected when a jumper component is moved.



#### [Notes and Restrictions]

- If the Reroute mode is activated, jumper processing is not performed regardless of this specification.

## Three-point rotation of component

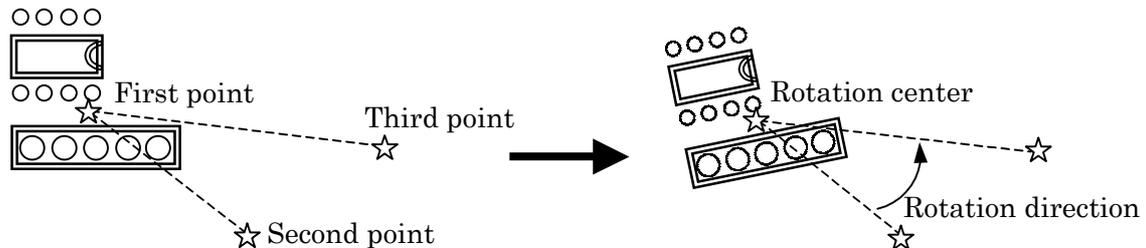
### [Function]

With Rev. 6.0, you can rotate a component by specifying three points. In the Three-point rotation mode, the component is rotated based on the following coordinates.

First point: Rotation center coordinates

Second point: The start point of rotation

Third point: The end point of rotation



## ● Improved component change and generation commands

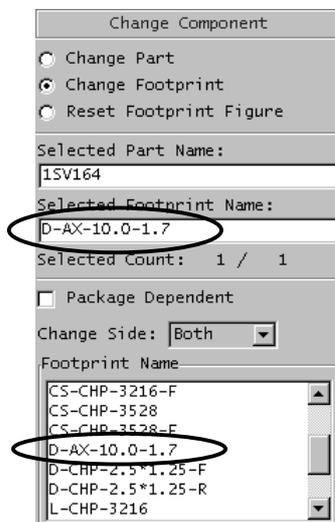
The following functions are added or improved for the component change and generation commands.

- Automatic scrolling of the change list
- “Do Not Change Footprint” option on changing part
- Specifying another footprint at part changing and component generation
- Improved operation on part changing and component generation
- Reset function for footprint shapes

## Automatic scrolling of the change list

### [Function]

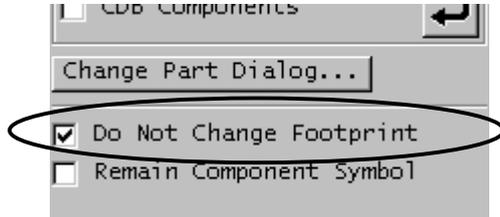
With Rev. 6.0, when a part or footprint is changed and the change list is the same as the selected component, the list is automatically scrolled and displays the component in the center of list.



## “Do Not Change Footprint” option on changing part

### [Function]

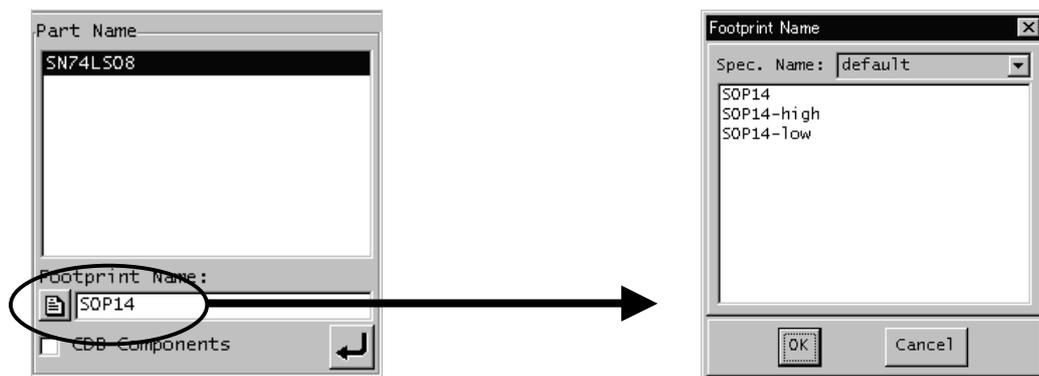
With Rev. 6.0, you can change a part while leaving the original footprint. When the “Do Not Change Footprint” option is activated, the original footprint and edited figures remain the same even when a part is changed.



## Specifying another footprint at part changing and component generation

### [Function]

With Rev. 6.0, you can specify a footprint other than default when changing a part or generating a component.



### [Notes and Restrictions]

- You can specify only footprints in the package of the component to be changed or generated.
- You cannot specify a footprint other than default for the printed component.

## Improved operation on part changing and component generation

### [Function]

If a package or footprint specified by a part is not in the PCB when changing a part or generating a component, Rev. 6.0 copies necessary information from CDB.

Rev. 6.0 displays a warning message after copying and displays execution results in the Query Data window.

If the package or footprint is not in CDB, an error message appears interrupting the process.

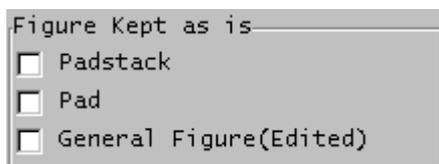
## Reset function for footprint shapes

### [Function]

With Rev. 6.0, the footprint shape reset mode is added for the component change command. This enables selection of an edited component from the PC board and resetting of the footprint shape (i.e. undo editing).



You can also specify In-component figures with saved shapes when the footprint shapes are reset.



### Reference

For options on the mode for figures with shapes to be saved, see “4-3 Component Operations •Added or improved CDB component update function/ •“Keep In-component Figure” option on footprint update.”

## ● Improved CDB component copy function

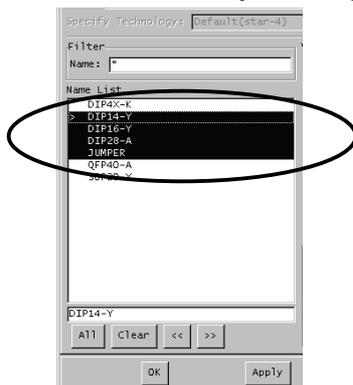
The following functions are improved for the command used to copy components from CDB.

- Selecting multiple lists
- Common dialog box for master file specification (common to the component update command)

## Selecting multiple lists

### [Function]

With Rev. 6.0, you can select multiple list items as when updating components from CDB. Select items by clicking them while touching the Ctrl or Shift key.

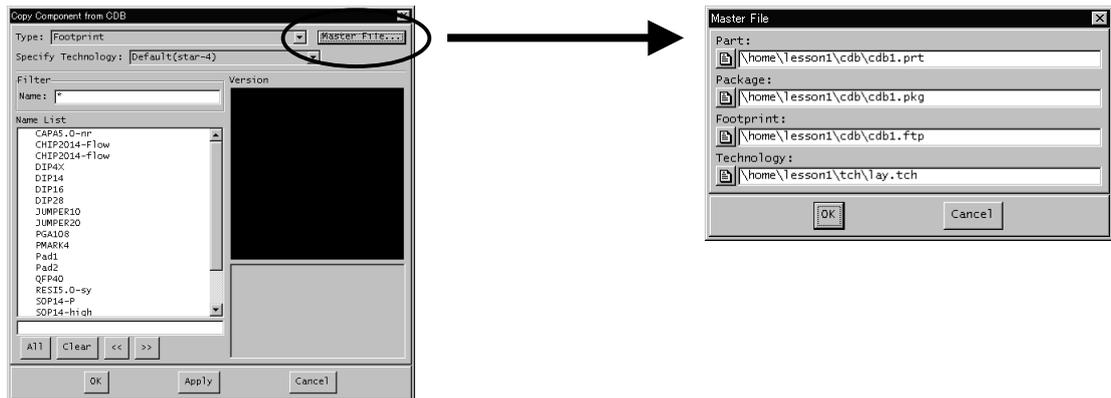


## Common dialog box for master file specification (common to the component update command)

### [Function]

With Rev. 6.0, the master file is not specified in the main dialog box but in a different dialog box.

Clicking **Master File...** in the upper right of the dialog box starts the Master File dialog box.



## ● Added or improved CDB component update function

The following functions are added or improved for the command to update components from CDB.

- Filter used to specify the select list version
- “Keep In-component Figure” option on footprint update

## Filter used to specify the select list version

### [Function]

With Rev. 6.0, the “version” option list is added in the filter frame. You can filter out data to select according to the following rules.

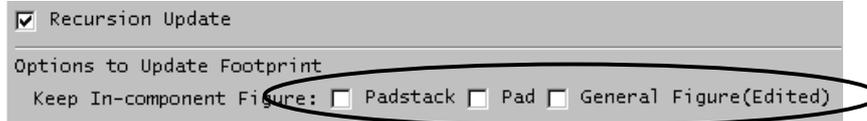


Version	Explanation
Unspecified	Displays all regardless of the versions.
Lower Than Master	Displays objects with higher master versions than local versions.
Different	Displays objects where master and local versions differ and objects where only local versions exist.

## “Keep In-component Figure” option on footprint update

### [Function]

With Rev. 6.0, you can specify In-component figures of which shapes are saved on footprint update. Select the check box corresponding to the In-component shapes to save below the “Options to Update Footprint” label.



Option	Explanation
Padstack	When the padstack check box is selected, all padstacks in the component are left as they are regardless of shape editing.
Pad	When the pad check box is selected, all pads (except the pads in padstack) in the component are left as they are regardless of shape editing.
General figure (edited)	The general figure means all editable figures on the PC board except padstack and pad. When the general figure (edited) check box is selected, all In-component general figures on the layer where shape editing is done are saved as they are.

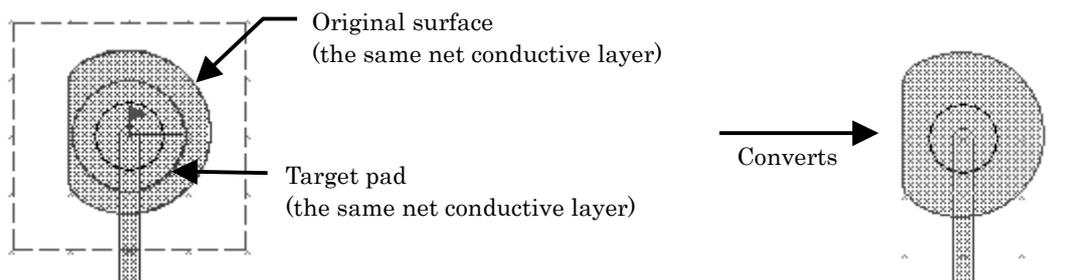
## ● Pad editing (supporting the same net surface loading)

### [Function]

With Rev. 5.0, there is a restriction that the surface data to load during pad editing should not be related to a net. In contrast, Rev. 6.0 can load a surface with net if the net is the same as that of the pad or padstack. This enables loading of a surface input with the Placement/Wiring Tool during pad editing.

### [Operation]

- (1) Select **Edit** → **Edit Pad** from the menu bar.
- (2) Set **[Edit Mode]** to **[Take in Surface]** and **[Layer to Edit]** to **[Conductive layer]** in the panel menu and select the layer containing the target pad from the list.
- (3) Specify a pad on the canvas.
- (4) Clicking **[Next Surface]** in the panel menu displays the original surface layer in **[Surface Layer to Take:]** as candidate.
- (5) Clicking **↵** converts.



## ● Reference change lock flag

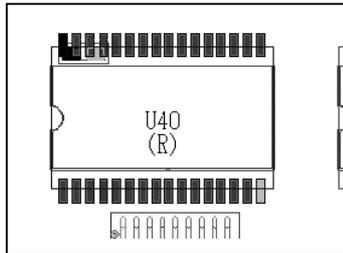
### [Function]

The reference change lock flag is added for Rev. 6.0 to prevent the changing of a component reference.

This helps to avoid changing a reference by mistake during PC board design.

When the reference attribute display is activated, Mark “(R)” indicating that the reference is locked is displayed for a component with a locked reference.

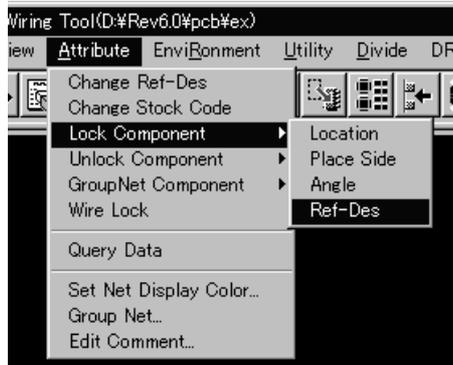
This can also be checked with the Query Data command. If the reference is locked, “ra\_lock” is “LOCKED.”



Because the reference change lock flag corresponds to the component reference fixing flag on the SD, this setting can be reflected with forward annotation and back annotation.

### [Operation]

- (1) Select a component with reference to lock.
- (2) Select **Attribute** → **Lock Component** → **Ref-Des** from the menu bar.



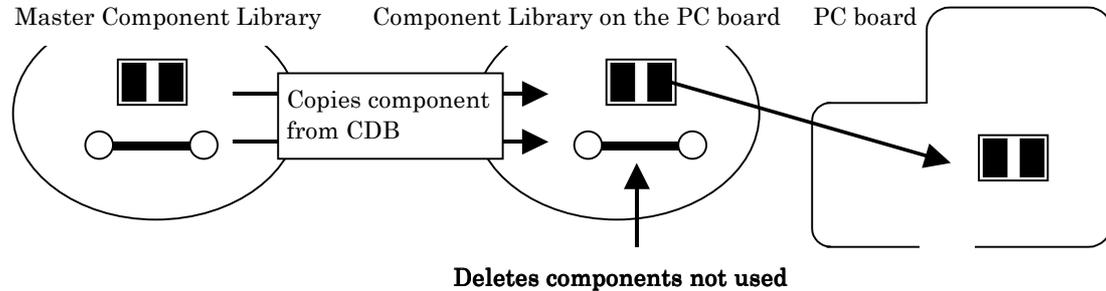
### [Notes and Restrictions]

- Mark “(R)” indicating a locked reference is not displayed for a component on the sub-PC board.
- When a PC board block from a sub-PC board is developed on the parent PC board, the reference lock setting done during sub-PC board editing is not reflected to the parent PC board. A warning message appears on development if the settings for the reference change lock flag are different between the sub-PC board and parent PC board.

## ● Function to delete components not used from the PC board

### [Function]

A function is added to delete the components copied from the CDB library to the PC board but not used on the PC board from the PCB database(PCB).

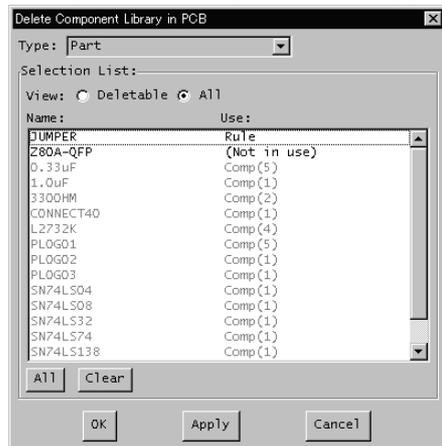


This improvement has the following effects.

- You can easily delete secret components before giving data to a subcontractor.
- You can re-copy component information with a changed design. (If you try to update components from CDB with a changed pin name or pin number, an error message “Different structure” appears and updating is not permitted.)
- You can minimize the size of the PCB database.

### [Operation]

- (1) Select **Utility** → **Delete Component Library in PCB** from the menu bar.
- (2) Select a library containing components to delete (part, package, footprint, padstack or pad) from **[Type]**.



- (3) After the components that can be deleted are displayed in black, click component names to delete.
- (4) Select **[Apply]**.

### [Notes and Restrictions]

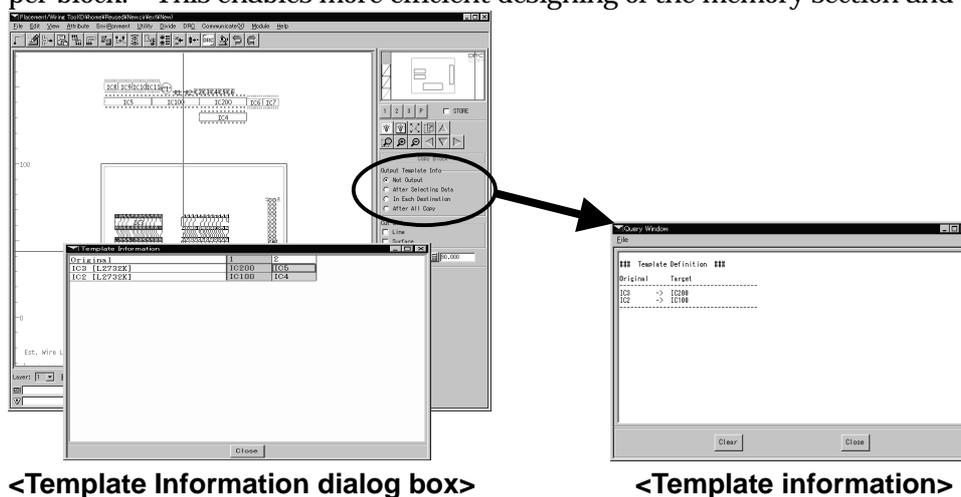
- This function does not support Undo/Redo.
- After executing this command, execute the Database Compaction Program (pcbcompact). Otherwise, the PCB database(PCB) size is not actually reduced.

# 4-4 Template Placement/Wiring Function



## [Function]

With Rev. 6.0, you can copy PC board components and patterns with the same part name per block. This enables more efficient designing of the memory section and other parts.



## [Operation]

- (1) Select **Edit** → **Copy Block** from the menu bar.
- (2) Select [Parameter] → [Template information output] from the panel menu.
- (3) Select [Noun to Cut].
- (4) Set [Rotation Pitch:] to rotate data at the time of copying.
- (5) Select an original (template) component and wiring by specifying an area, and then select [Data End] from the Assist Menu.
- (6) Specify a drag reference point for copying on the canvas.
- (7) The Template Information dialog box appears. Select a copy destination component in the dialog box.  
(Light blue indicates the selected component group.)
- (8) Specify a copy destination, and then select [Data End] from the Assist Menu.  
To select another component group, go back to (7).  
(Red indicates processing completion.)

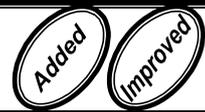
## [Notes and Restrictions]

- The copy destination component should satisfy one of the following rules.
  - The component has the same part name as that of the original component
  - The component is not placed or is outside of the board outline
  - Connection information for the original component is the same as that of the pin (the temporary net is not within the range.)
  - The component is not position locked
  - If the angle is locked for the component, the angle should be the same as that of the original component.
  - If the placement side is locked, the side should be the same as that of the original.

---

## 4-5 Divided/Reused design

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The following functions are added or improved for the Board Split command related to the divided and reused design.

- PC board block load function by specifying the reference point
- The reference point and vertex in the divided area are added to the candidate for the same point
- Dashed line non-connected net search
- Loading a reused PC board by specifying a directory path
- Change in the way the drag reference point for moving by dragging is specified
- Loading the same PC board into multiple locations
- Design rule difference extraction function
- Improved net name processing on PC board development

### ● PC board block load function by specifying the reference point

#### [Function]

You can load PC board blocks by specifying coordinates other than the origin (0,0) as the reference point.

#### [Operation]

- (1) Select **Divide** → **Divide** from the menu bar.
- (2) Select [Enter Base Point] from the Assist Menu and specify the reference point on the canvas.
- (3) Execute [Load Nesting] or [Load Reused Block Template].

#### [Notes and Restrictions]

- Until you click **OK** in the Technology Connector dialog box, the reference point for the PC board to load is the origin.

### ● The reference point and vertex in the divided area are added to the candidate for the same point

#### [Function]

With Rev. 6.0, you can search the divided/split area while regarding the reference point and a vertex as the same point.

## ● Dashed line non-connected net search

### [Function]

With Rev. 5.0, you cannot search for a component in the divided/split area before development or a non-connected net for a component at layout (net displayed with dashed lines) by using the Input Wire command.

With Rev. 6.0, you can search a non-connected net displayed with dashed lines and display its cursor ID.

You can extend the line from the start or end point of the non-connected net (dashed line) and retract it to the start and end points.

### [Notes and Restrictions]

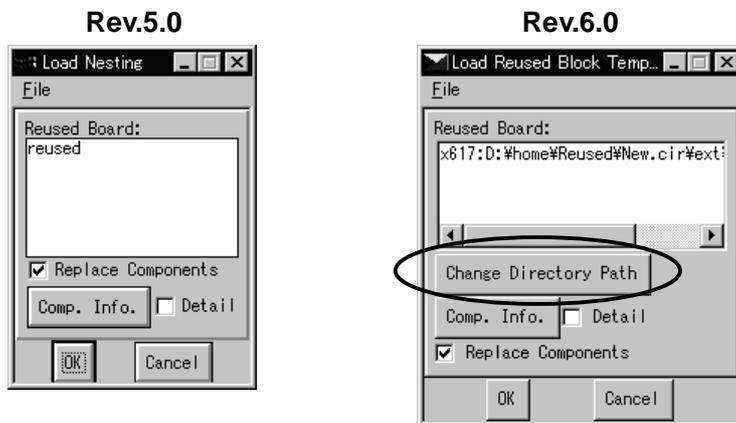
- While a route is being specified, the rubber band between the point last specified and the end point is not displayed.

## ● Loading a reused PC board by specifying a directory path

### [Function]

With Rev. 5.0, reusable PC board data should be in the directory containing the target PC board data or it cannot be loaded.

With Rev. 6.0, you can change a directory path for the reusable PC board data when loading PC board data.



## ● Change in the way the drag reference point for moving by dragging is specified

### [Function]

With Rev. 5.0, when moving the divided/split area, the reference point for the divided/split area is the drag reference point.

With Rev. 6.0, the drag reference point is a point specified when selecting the divided/split area to drag.

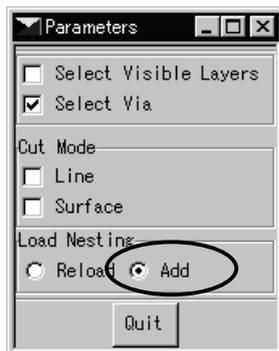
## ● Loading the same PC board into multiple locations

### [Function]

With Rev. 6.0, you can load the same PC board into multiple locations and develop it.

### [Operation]

- (1) Select **Divide** → **Divide** from the menu bar.
- (2) Click a parameter from the panel menu, and then set [Load Nesting] to [Added].
- (3) Specify a PC board data with [Load Nesting].
- (4) Execute [Load Nesting] and then [Expand].



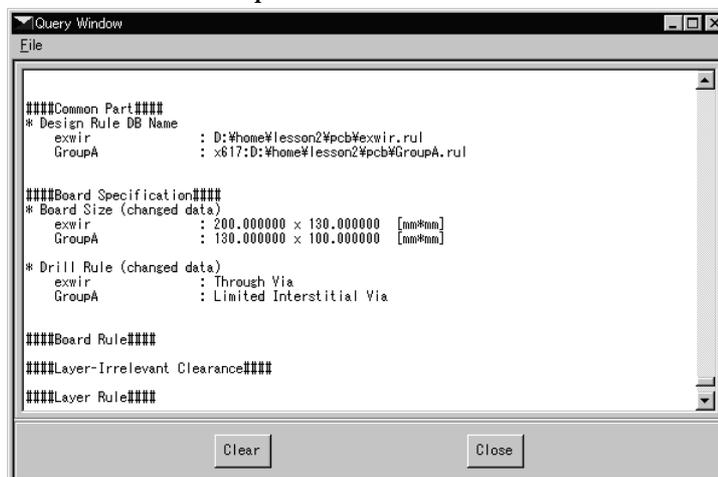
### [Notes and Restrictions]

- [Load Nesting] does not support this function.

## ● Design rule difference extraction function

### [Function]

With Rev. 6.0, you can extract differences between design rules for the PC board being edited and those for the specified PC board to divide or reuse.



## ● Improved net name processing on PC board development

### [Function]

Processing for the net name of the pattern to be developed in the “net processing mode” [Divide] is improved as follows.

#### <Processing for the net name of the component pin developed>

Net processing	Rev.5.0	Rev.6.0
Merge (no change)	The net names are copied to the destination PC board as-is.	The net names are copied to the destination PC board as-is.
Divide (no change)	The net names are renumbered in the format of \$BN00000[number] on the destination PC board.	The net names are renumbered in the format of \$BN00000[number] on the destination PC board.

#### <Processing for the net name of the pattern developed>

Net processing	Rev.5.0	Rev.6.0
Merge (no change)	If the net name exists in the destination PC board, the net name is employed. If not, the net is copied as temporary net.	If the net name exists in the destination PC board, the net name is employed. If not, the net is copied as temporary net.
Divide (no change)	The sub-net pattern connected to developed component pin is renumbered in the format of \$BN00000[number]. For others, if the net name exists in the destination PC board, the net name is employed. If not, the net is copied as temporary net.	The sub-net pattern connected to developed component pin is renumbered in the format of \$BN00000[number]. For others, if the net name exists in the destination PC board, the net name is employed. If not, the net is copied as temporary net.

# 4-6 Wiring Command



The following functions are added or improved for the wiring edit function.

- Improved online DRC processing (Wire Input and Wire Move)
- Improved extension/retraction (Wire Input)
- Improved From-To field for design without Interstitial Via (Wire Input)
- Function added to batch-connect multiple pins (Wire Input)
- Function added to display the wiring length during wiring (Wire Input)
- Target layers and figures added for template routing (template routing)
- Function to generate a fillet on a line with two vertexes
- Topology rule display
- Supporting square lines [Optional]

## ● Improved online DRC processing (Wire Input and Wire Move)

### [Function]

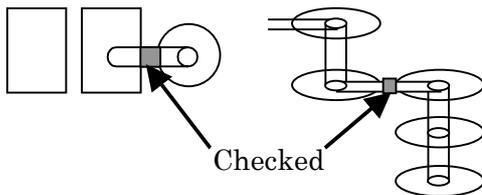
Online DRC during execution of the Wire Input and Wire Move command is improved as follows:

- Supporting same-net clearance check (Wire Input and Wire Move)
- Supporting resist check (Wire Input and Wire Move)
- Supporting actual figure check (Wire Input)

### Supporting same-net clearance check (Wire Input and Wire Move)

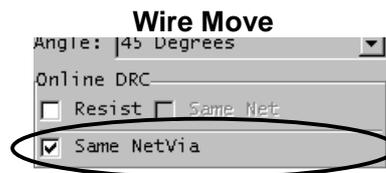
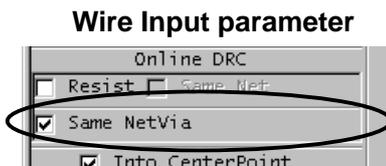
### [Function]

You can check clearance to the same net Via and pin with online DRC when inputting or moving a Via. The supporting commands are “Wire Input” and “Wire Move.”



### [Operation]

Select [Same Net Via] in [Parameter] for the Wire Input command or the panel menu for the Wire Move command.



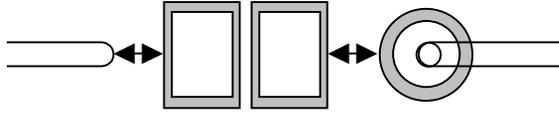
### [Notes and Restrictions]

- The spread function for the Wire Input command and the pushing-aside function for the Wire Move command do not support this check.

## Supporting resist check (Wire Input and Wire Move)

### [Function]

You can check clearance to the resist with online DRC when inputting or moving a line or Via. The supporting commands are “Wire Input” and “Wire Move.”



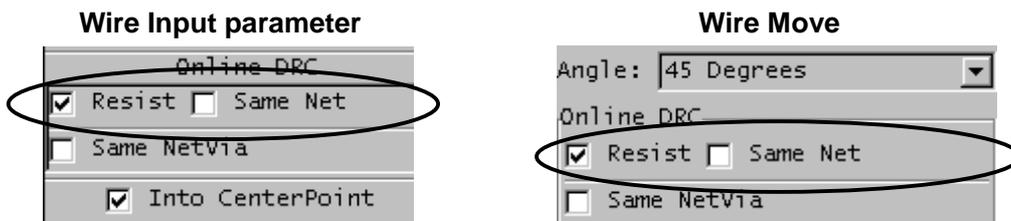
### Reference

The Surface Edit command supports similar functions. For this command, see “4-7 Editing Surface •Resist support (surface input).”

### [Operation]

Select [Online DRC]→[resist] in [Parameter] for the Wire Input command or the panel menu for the Wire Move command.

To check against the same-net resist, select [Same Net].



### [Notes and Restrictions]

- The spread function for the Wire Input command and the pushing-aside function for the Wire Move command do not support this check.

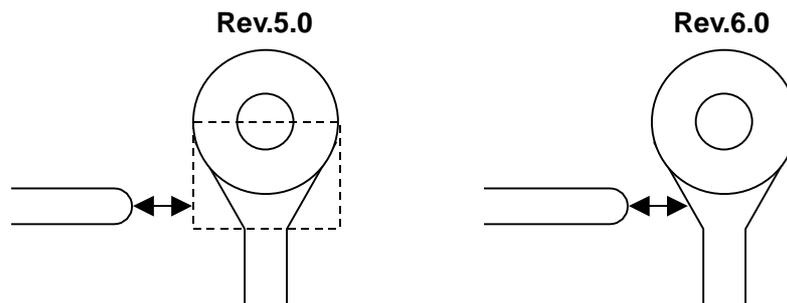
## Supporting actual figure check (Wire Input)

### [Function]

On Rev. 5.0 or older, online DRC checks the clearance between a fillet or pad to the enclosing rectangle during Wire Input.

With Rev. 6.0, online DRC perform clearance check on an actual figure during Wire Input.

This enables input of a pattern as near as possible to a fillet or pad. The supporting command is Wire Input.



## ● Improved extension/retraction (Wire Input)

### [Function]

Extension/retraction processing during execution of the Wire Input command is improved as follows:

- Supporting oblong pad in center extension/retraction
- Pin priority on extraction
- Padstack priority on extraction
- Function to select the next candidate for retraction
- Improved padstack retracting in the single layer mode

### Supporting oblong pad in center extension/retraction

#### [Function]

With Rev. 5.0 or older, you can extract or retract only to/from the oblong pad center.

With Rev. 6.0, the wiring input parameter, [Into Center Point], becomes valid for oblong pad, too. This enables extraction or retraction to/from a point other than the oblong pad center.

### Pin priority on extraction

#### [Function]

With Rev. 5.0 or older, the non-connected net has priority over wiring pattern and pin if a wiring pattern or pin selected for extraction overlaps a non-connected net.

With Rev. 6.0, the wiring pattern and pin has priority over non-connected net. This facilitates extraction from a pin that overlaps a non-connected net.

### Padstack priority on extraction

#### [Function]

With Rev. 5.0 or older, if a trap area selected for extraction contains a padstack and connected line pattern, one of them is selected randomly. Therefore, when you try to select a padstack, a line might be selected, leaving a short segment in the padstack after changing the route.

With Rev. 6.0, the padstack has priority over line pattern. This reduces short segments left in the padstack after changing the route.

## Function to select the next candidate for retraction

### [Function]

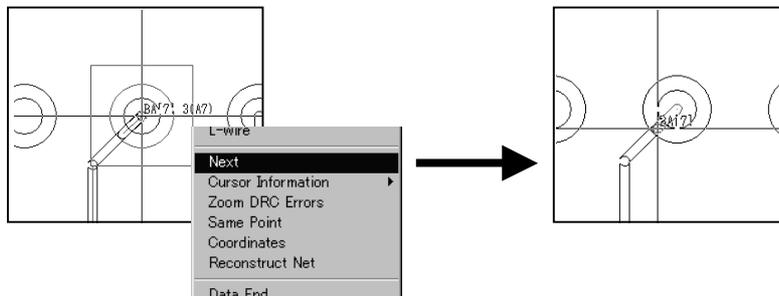
With Rev. 5.0 or older, if a trap area selected for retraction contains a padstack and connected line pattern, the padstack is always selected and line selection is not possible.

With Rev. 6.0, you can switch the target by selecting [Next].

This enables retraction of the wiring pattern into a line intentionally extracted from a padstack.

### [Operation]

- (1) While a figure to retract is highlighted during wiring input, select **Next** from the Assist Menu.
- (2) Select a line into which the figure is retracted.



## Improved padstack retracting in the single layer mode

### [Function]

With Rev. 5.0 or older, when you want to extract a line pattern from a padstack but the padstack is impossible to extract, the single layer mode is changed to the active layer.

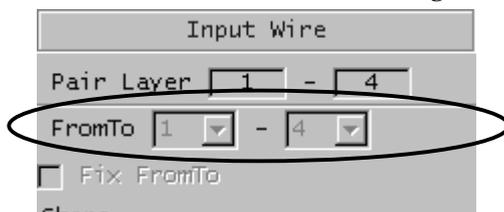
With Rev. 6.0, a padstack that is impossible to extract from the active layer cannot be selected in the single layer mode.

This prevents the single layer mode from automatically changing to active.

## ● Improved From-To field for design without Interstitial Via (Wire Input)

### [Function]

If the design rule set “Inter-layer Via = None,” the From-To field in the panel menu is shaded and unavailable during execution of the Wire Input command.



## ● Function added to batch-connect multiple pins (Wire Input)

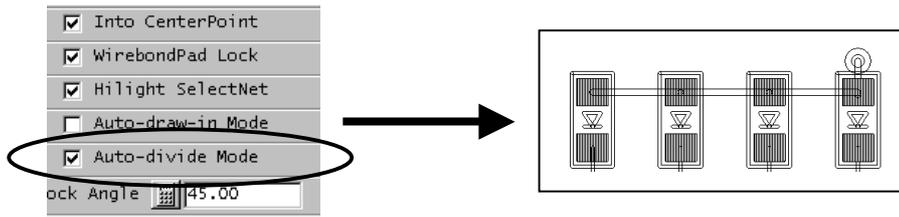
### [Function]

A function is added to split a line and connected it to a pad or padstack when data is fixed if a line pattern input with the Wire Input command goes through a pad or padstack on the same net.

This enables simultaneous connection of multiple pads or padstacks.

### [Operation]

- (1) Select [Parameter]→[Online DRC]→[Auto-divide Mode].
- (2) Place wiring going through a pad or padstack with the same net.



## ● Function added to display the wiring length during wiring (Wire Input)

### [Function]

A function is added to display wiring length and other information on line patterns being input in the Wiring Length Graph dialog box.

If you select [Display Chart] in the panel menu for the Wire Input command, the total wiring length of the currently input line pattern and line patterns on the input net is displayed in the dialog box during line pattern input.

## ● Target layers and figures added for template routing (template routing)

### [Function]

With Rev. 6.0, template routing becomes possible for the following layers and figures.

#### <Layer and figure supporting template routing>

Layer	Wiring Keep-out layer, Via Keep-out layer, Only Wire Keep-out layer and figures on the layout area layer
Figure	Padstack, pad and hole (circle, rectangle and oblong)

### [Notes and Restrictions]

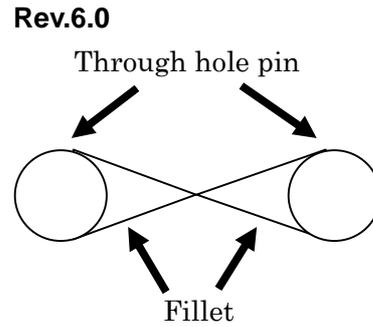
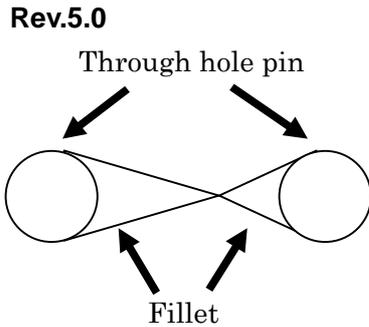
- These layers or figures can be selected only when the [Area Specification] mode is active.
- You cannot perform template routing for inner outline of the closed line on a layer other than a conductive layer.
- Template routing for the layout area always generates line within the area. You cannot generate a line outside of the layout area.

## ● Function to generate a fillet on a line with two vertexes

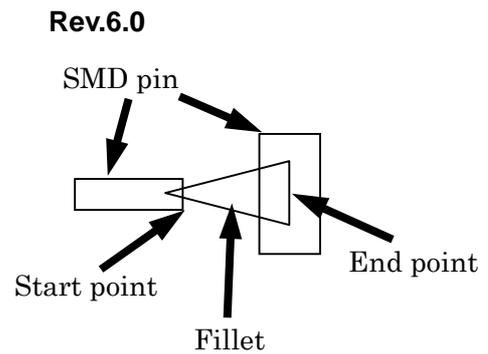
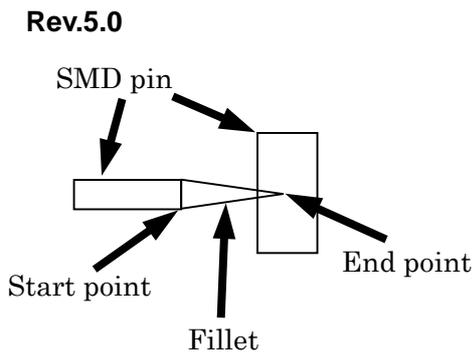
### [Function]

The Rev. 5.0 Wiring Post-processing command generates or changes a fillet from the start point of line. Therefore, sometimes it is impossible to generate a fillet at the end point or one generated at the end point side might be short.

Rev. 6.0 generates a fillet after shortening fillets at the start and end points by the same amount when the line has two vertexes.

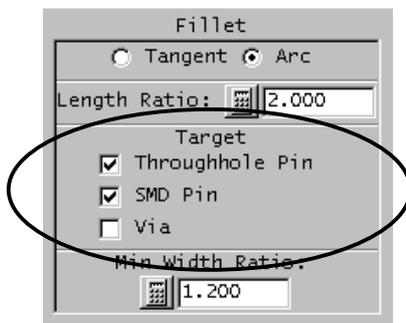


If fillets cannot be generated at the edges of a line with two vertexes, a wider fillet is generated.



### [Notes and Restrictions]

- When a fillet is generated, the check boxes in “Target” of the Wiring Post-processing command parameters are referred to. On the other hand, they are not referred to when a fillet is changed.



## ● Topology rule display

### [Function]

With Rev. 6.0, you can display topology rules in the Cursor Information dialog box during wiring-related command execution. You can design while checking the displayed pin pair maximum and minimum wiring lengths and notes on topology design (comment).

### [Notes and Restrictions]

- Even if the topology rule is not set, the pin pair rule, maximum and minimum wiring lengths are displayed in the Cursor Information dialog box if the pin pair rule is set.
- Use the PreTransmission or SPECCTRAQuest for the System Designer to set topology rules.

## ● Supporting square lines [Optional]

### [Function]

You can input and move a square line by using the Wire Input and Wire Move command for the Placement/Wiring Tool as HIC design is supported.

### [Notes and Restrictions]

- To execute the square line input function, you need a license for an HIC design module.
- A square line can be input only in the horizontal or vertical direction.

## 4-7 Editing Surface



The following functions are added or improved for the surface editing function.

- Resist support (surface input)
- Function added to cut out figures on the non-conductive layer (figure cutout)
- Improved mesh function (putting and editing mesh)

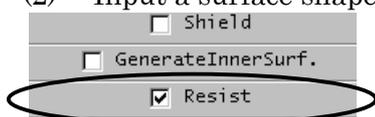
### ● Resist support (surface input)

#### [Function]

A parameter is added to generate and input a surface considering clearance to resist figures. With Rev. 5.0, you have to cut out a resist shape after inputting a surface. With Rev. 6.0, surface shape considering resist interference can be created only with the surface input command.

#### [Operation]

- (1) Select [Parameter]→[Figure cutout]→[Resist] for the surface input command.
- (2) Input a surface shape.



#### [Notes and Restrictions]

- If a resist does not have different net padstack from the input surface, the resist is not regarded as an inhibited figure. This may cause an Area DRC error.

### ● Function added to cut out figures on the non-conductive layer (figure cutout)

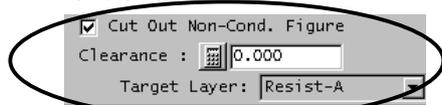
#### [Function]

With Rev. 6.0, you can cut out the conductive layer surface with a non-conductive layer figure.

This enables editing of an input surface to shape considering interference with resists, metal masks and other elements.

#### [Operation]

- (1) Select [Parameter] → [Cut Out Non-Cond. Figure] for the surface input command, and then set a clearance and target non-conductive layer.
- (2) Click the figure cutout icon in the panel menu and specify a surface and figure to cut out.



#### [Notes and Restrictions]

- To cut out a resist figure, the larger of the specified clearance and the design rule clearance is employed.
- If the target layer is set as visible layer, a figure to cut out is searched for in both of the all layer and single layer modes.

## ● Improved mesh function (putting and editing mesh)

The following functions are added for the mesh-related commands used for surface input.

- Design rule reference function
- Mesh editing function

### Design rule reference function

#### [Function]

Rev. 6.0 features a function to define the cutout figure limit as a design rule and put mesh on a surface according to the limit.

This enables generation of a mesh plane considering limit at the time of photo output. The supporting command is the Put Mesh command.

#### [Operation]

- (1) Set mesh cutout figure limit as a design rule.
- (2) Select a diameter of cutout figure from the list in the panel menu [Mesh parameter] for the Input Surface command or input a numeric value by using the calculator icon or keyboard (the input numeric is adjusted according to the limit.)
- (3) Put mesh on the surface

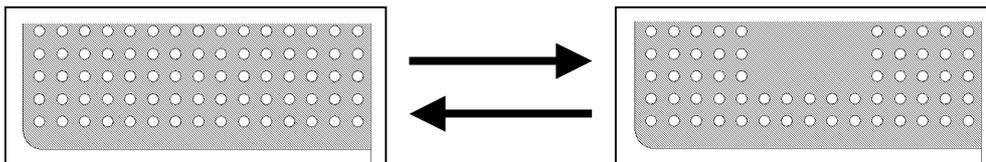
#### Reference

For setting design rules, see “3-3 Design Rule Editing Tool • Setting new rules • Mesh cutout figure limit.”

### Mesh editing function

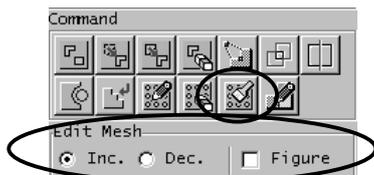
#### [Function]

A function is added to increase or diminish cutout figures on generated mesh planes. The Edit Mesh command is added for this purpose.



#### [Operation]

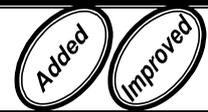
- (1) Select [Edit Mesh]  from the panel menu [Command] for the Input Surface command.
- (2) Select a mesh plane and specify a location where a cutout figure is added or deleted from.



#### [Notes and Restrictions]

- You cannot add a cutout figure to a position within the minimum wiring pattern width (if this is not set, the wiring pattern width) specified by the design rule from a surface outline and window.

## 4-8 Generating Shield



The following functions are added or improved for the surface editing function.

- Improved pattern shape generation
- Added function to generate a shield surface
- Added function for multiple net shields (wiring post-processing)

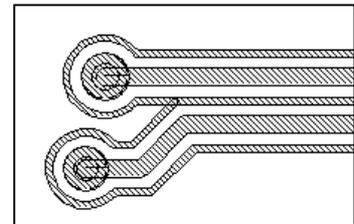
### ● Improved pattern shape generation

#### [Function]

A shielding shape automatically generated and a retraction shape generated by retraction from shielding to Via or surface are improved.

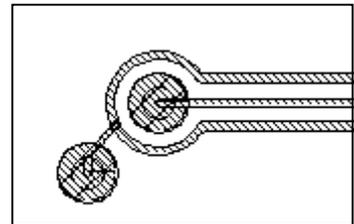
#### <Improvement in generated pattern shapes>

If the interval between lines requiring shield can contain only one shield pattern, Rev. 5.0 generates two overlapped shield patterns. In contrast, Rev. 6.0 generates one shield pattern and prevents overlapping.



#### <Improvement in retraction pattern shape >

While retraction is performed per 90° on Rev. 5.0, this can be performed in 45° units on Rev. 6.0.



## ● Added function to generate a shield surface

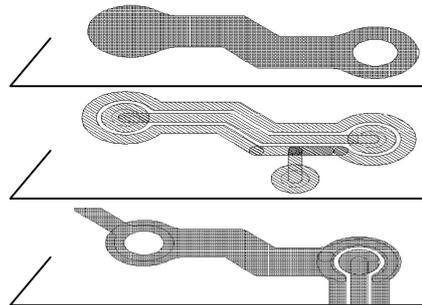
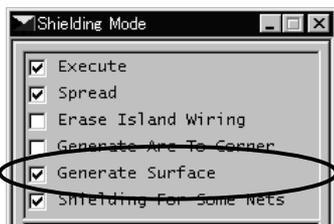
### [Function]

A function is added to automatically generate a shield surface on the layer adjacent to the line that needs a shield. The supporting commands are as follows:

- Input Wiring
- Move Wiring
- Delete Wiring
- Wiring Post-processing

### [Operation]

- (1) Select the [Generate Surface] check box in the dialog box started by selecting **Environment** → **Shielding Mode** on the menu bar.
- (2) Edit a line requiring a shield.



### [Notes and Restrictions]

- If there is a figure causing a DRC error in relation with the generated shield surface, shield surface figure cutout is not performed.
- Retraction is not performed from the generated shield surface and the surface become the island shield surface.
- Selecting [Erase Island Wiring] in the Shielding Mode dialog box deletes only island shield lines and not island shield surfaces.

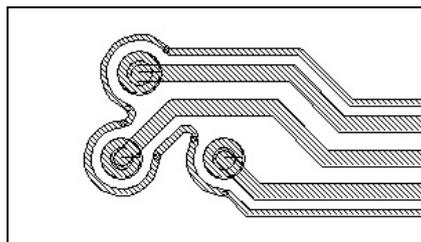
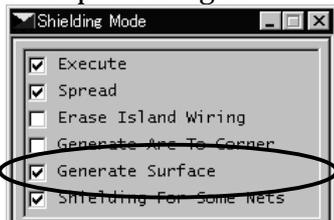
## ● Added function for multiple net shields (wiring post-processing)

### [Function]

A function is added to simultaneously shield multiple lines that need shielding. The supporting command is the Wiring Post-processing command.

### [Operation]

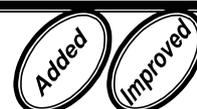
- (1) Select the [Shield For Some Nets] check box in the dialog box started by selecting **Environment** → **Shielding Mode** on the menu bar.
- (2) Generate a shield by specifying multiple patterns in an area with the Wiring Post-processing command.



### [Notes and Restrictions]

- The generated shield pattern is correlated with one of the selected nets. Therefore, editing another net does not influence the shield pattern.

## 4-9 Edit Command



The following functions are added or improved for the Edit command.

- Added or improved functions for the Copy/Move command
- Rule reference on changing padstacks
- Square line support

### ● Added or improved functions for the Copy/Move command

The following functions are added or improved for the Copy/Move command.

- Function added to select only Vias
- Moving a line while maintaining the shield attribute
- Referring to the pattern width limit rule
- Copying without maintaining the lock attribute
- Copying without maintaining the test point attribute

### Function added to select only Vias

#### [Function]

A mode is available to select only Vias when [Select Via] is selected for the Copy or Move command. This realizes efficient selecting.



On: Selects only Vias.

Off: Select Vias and other figures.

### Moving a line while maintaining the shield attribute

#### [Function]

When a shield line is moved on Rev. 5.0, the shield attribute is cleared.

Rev. 6.0 moves such a line maintaining the shield attribute if possible.

#### [Notes and Restrictions]

- If a line is moved to the non-conductive layer, the shield attribute is deleted. (The line becomes an ordinary line.)
- When the [Fix Net] check box is cleared and a different net is added to a moved line, the line becomes unrelated to the shielded line.
- When copying a line, the shield attribute is cleared regardless of the [Fix Net] setting.

## **Referring to the pattern width limit rule**

### **[Function]**

When a line or surface is moved or copied from a non-conductive layer to a conductive layer on Rev. 5.0, a line or surface with a width not permitted by the wiring width limit can be input on the conductive layer because the pattern width limit on the conductive layer is ignored.

Rev. 6.0 refers to the pattern width limit rule when moving or copying an object to the conductive layer. If you try to move or copy an illegal pattern, the message,

“224174: It violates pattern width limitation.”

appears to attract your attention.

### **[Notes and Restrictions]**

- While a message appears when the line width or the outline width for the surface is illegal, the filling width of surface is not checked.
- Copying and moving is performed even when a message appears. You need to copy or move later.

## **Copying without maintaining the lock attribute**

### **[Function]**

When a pattern with the lock attribute is copied on Rev. 5.0, the copy destination pattern also has the lock attribute. On Rev. 6.0, the copy destination pattern does not have the lock attribute in such a case.

### **[Notes and Restrictions]**

- To copy a figure while maintaining the lock attribute, use the Template Placement/Wiring command.

## **Copying without maintaining the test point attribute**

### **[Function]**

When a Via with the test point attribute is copied on Rev. 5.0, the copy destination Via has the test point attribute. On Rev. 6.0, the copy destination Via does not have the test point attribute in such a case.

This avoids setting the test point attribute to a Via by mistake.

In short, the test point attribute can be added only using the Test Point Generation command.

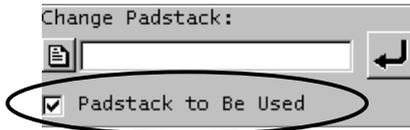
### **[Notes and Restrictions]**

- When a Via is moved, the attribute is maintained.

## ● Rule reference on changing padstacks

### [Function]

With Rev. 6.0, you can switch whether to refer to the used padstack. When the “Padstack To Be Used” check box is selected, the padstack cannot be changed to the default, qualified or other unusable padstacks.



## ● Square line support

### [Function]

You can input a square line on Rev. 6.0 as HIC design is supported. The following commands for the Placement/Wiring Tool function are explained below according to the limits on square line operation.

#### ●Edit Line

- In the [Divide] mode, the divided line maintains the square line attribute.
- In the [Merge] mode, a tangent arc is not generated.
- In the [Merge] mode, the connected line will be a circle line if the other is a circle line.

#### ●Copy/Move

- If a square line is selected, rotation is not performed unless the rotation angle is a multiple of 90. (An error message, “Cannot input a line with square pen type in the direction other than vertical and horizontal.” appears.)
- If the angle is not vertical and horizontal, the square line on the non-conductive layer is not copied nor moved.  
(An error message, “Cannot input a line with square pen type in the direction other than vertical and horizontal.” appears.)

#### ●Move Block

- If a square line is selected, rotation is not performed unless the rotation angle is a multiple of 90. (An error message, “Cannot input a line with square pen type in the direction other than vertical and horizontal.” appears.)
- The [Stretch Line] mode is invalid for a square line and is split.

#### ●Divide

- The square line with other than a vertical and horizontal angle is developed as a circle line.

### [Notes and Restrictions]

- To execute the square line input function, you need a license for an HIC design module.

# 4-10 Area DRC



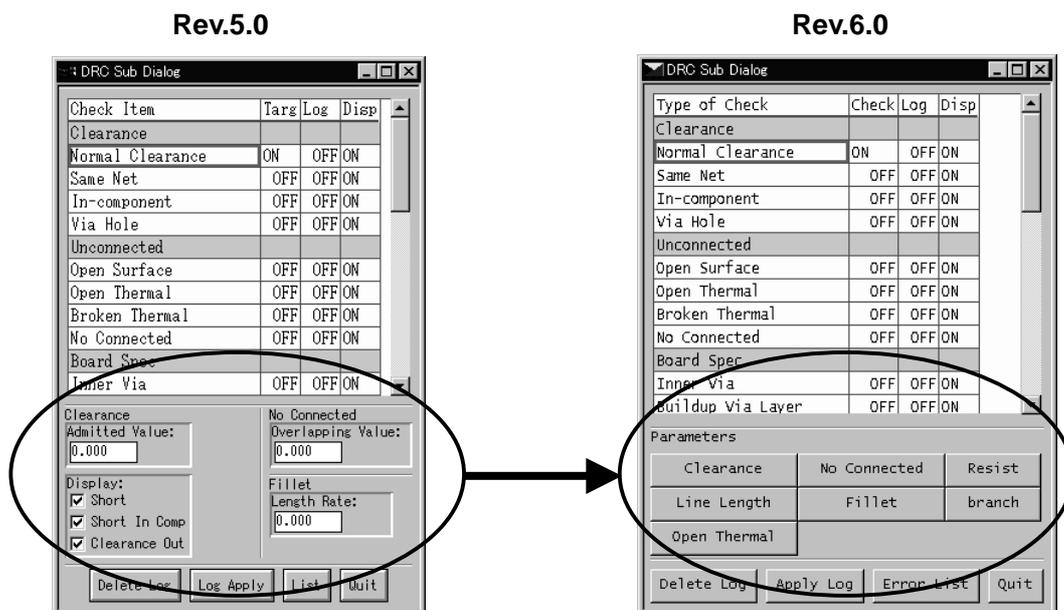
The following functions are added or improved for the Area DRC command.

- Improved DRC Sub dialog box
- Improved non-connection thermal check
- Improved non-connection check
- Improved Antenna Via check
- Improved resist check
- Improved fillet check
- Improved wiring width check
- Improved topology check
- Line length check
- Pin pair group maximum and minimum wiring length check
- Electrical net maximum and minimum wiring length check
- Confirmation dialog box for all area execution
- Interrupting Area DRC

## ● Improved DRC Sub dialog box

### [Function]

The [DRC Sub dialog box] has been improved so that you can start dialog boxes to set details on clearance check, non-connection check, resist check, fillet check, line length check and topology check from this dialog box.

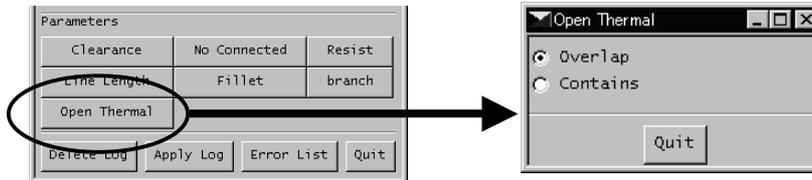


## ● Improved non-connection thermal check

### [Function]

Rev. 5.0 checks if a thermal hole overlaps a surface and does not cause an error if they overlapped slightly.

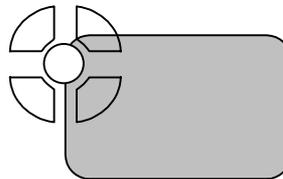
Rev. 6.0 checks if a thermal hole overlaps a surface and if the surface contains the thermal hole.



Overlap check:  
Checks if a thermal hole overlaps a surface (same as Rev. 5.0)



Does not cause an error.



Containing check:  
Checks if the surface contains the thermal hole



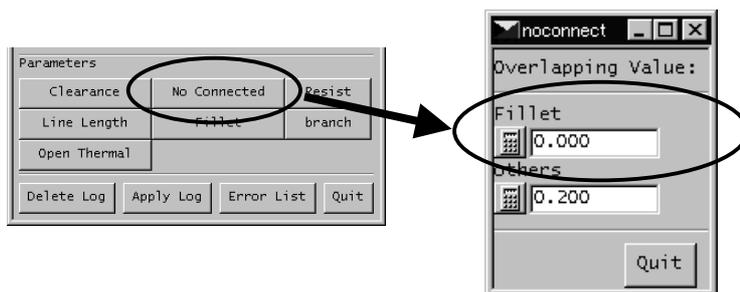
Causes an error.

## ● Improved non-connection check

### [Function]

With Rev. 6.0, you can set an overlap tolerance for fillet and perform a check. A figure with a width smaller than the overlap tolerance is not checked.

This reduces unnecessary errors and facilitates detection of errors that require action.



Fillet overlapping width

Checks if the overlapping width exceeds the overlap tolerance for fillet.

### [Notes and Restrictions]

- This checks the relationship between individual figures. Therefore, a DRC error occurs even if you reinforce a small overlapping area by inputting another figure.

## ● Improved Antenna Via check

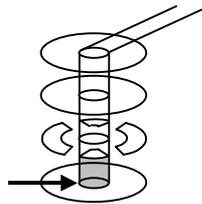
### [Function]

Up to Rev. 5.0, an error occurs against a Via with an antenna due to the limit on combinations of interstitial Vias. This error occurs even on Vias that do not need modification.

With Rev. 6.0, check is performed considering the limit on combinations of interstitial Vias defined by a design rule. This reduces unnecessary errors and facilitates detection of errors that require action.

Limit on combination of interstitial Vias

1 to 4



An error does not occur.

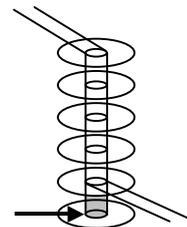
Limit on combination of interstitial Vias

1 to 2

2 to 5

5 to 6

1 to 6



An error does not occur.

### [Notes and Restrictions]

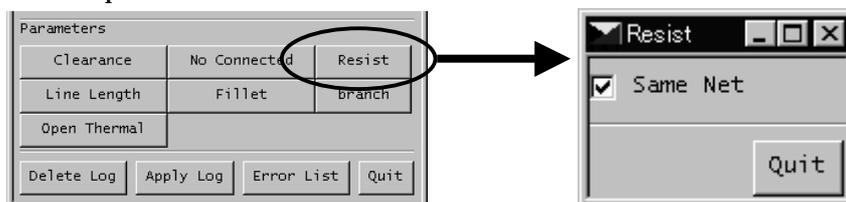
- If the limit on combinations of interstitial Vias exists, a check is performed while referring to the limit. If the limit does not exist, check is performed as with Rev. 5.0. In the latter case, Via and other objects thermally connected with inner layers all cause errors.

## ● Improved resist check

### [Function]

With Rev. 5.0 or older, a check is performed differently for resists in the padstack and those in the component or PC board. To be precise, a check is performed without considering the connection to line or surface for resists in the component or PC board. Therefore, an unnecessary error occurs at a point where a line or surface overlaps a resist in the component or PC board.

With Rev. 6.0, the check is made uniform to be performed on all resists in the padstack, component and PC board while considering the connection of the line or surface to check. This reduces unnecessary errors and facilitates detection of errors that require action.



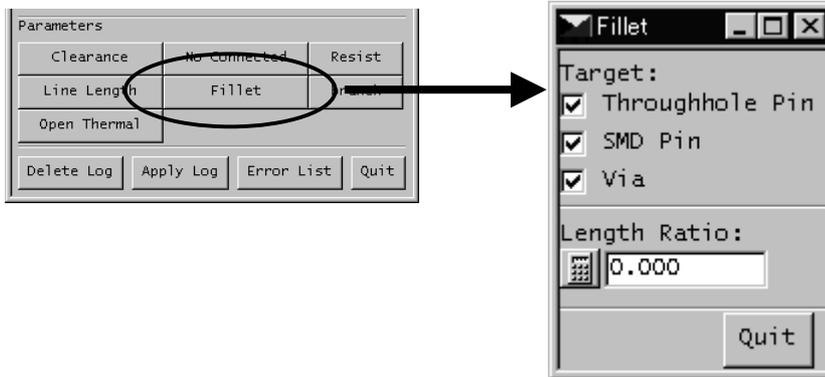
## ● Improved fillet check

### [Function]

Because Rev. 5.0 checks all pads and padstacks, a point where you did not generate a fillet intentionally causes an error.

With Rev. 6.0, you can select objects to check per connection target.

This reduces unnecessary errors.



### [Notes and Restrictions]

- Connection target setting is valid only for checks. Error mark deletion deletes all fillet check error marks regardless of this setting.

## ● Improved wiring width check

### [Function]

Rev. 5.0 checks only whether the maximum and minimum wiring widths are respected.

In addition, Rev. 6.0 checks if the design rule and wiring pattern width limit is respected.

## ● Improved topology check

### [Function]

The following functions are added or improved for the topology check.

- Recognizing the point where the wiring width changes as junction
- Recognizing a Via as junction
- Enhanced reference function for branch method errors

### [Notes and Restrictions]

- To set the topology rule, use the PreTransmission or SPECCTRAQuest for the System Designer.

### Recognizing the point where the wiring width changes as junction

#### [Function]

Rev. 6.0. enables performing of a check while regarding a point on the PC board where the wiring width changes as junction. This enables a check of the details at the point where the impedance changes.

### Recognizing a Via as junction

#### [Function]

Rev. 6.0. enables performing of a check while regarding a Via as junction. This enables a check of the details at the point where the impedance changes.

### Enhanced reference function for branch method errors

#### [Function]

Rev. 6.0 also outputs the following information.

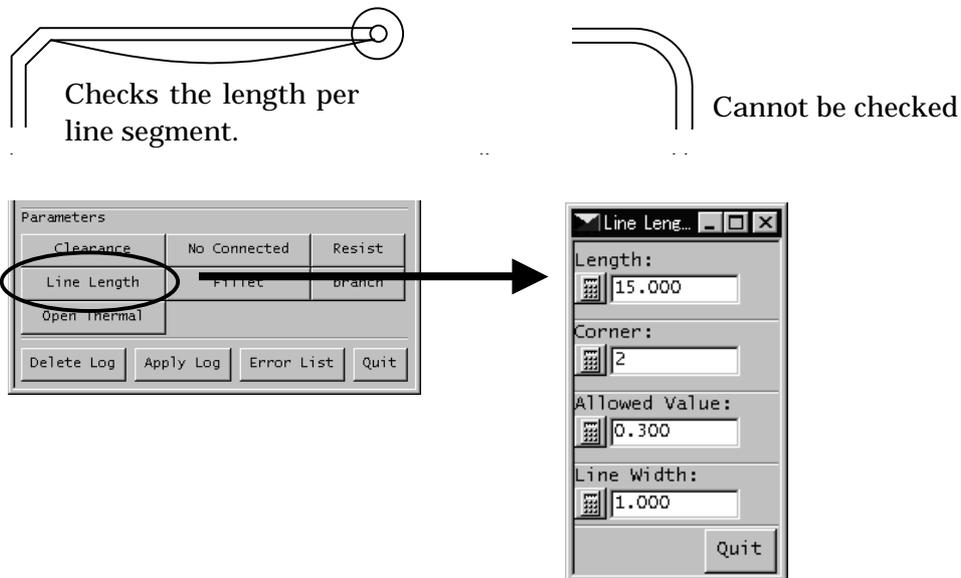
- Net name
- Electrical net name (for electrical net operation only)
- Topology rule
- Current wiring status
- Whether to regard Via as junction

## ● Line length check

### [Function]

Rev. 6.0 has a new function to check line length per line segment.

An error occurs to inform you of a line segment longer than the specified length.



### [Notes and Restrictions]

- If the set length is 0 (default), a check is not performed.
- If the set wiring width is 0 (default), a check is not performed.
- While you can check line segments making up a straight line, you cannot check lengths of arc, tangent arc or fillet.

## ● Pin pair group maximum and minimum wiring length check

### [Function]

If you have set the maximum and minimum wiring lengths for pin pair groups, you can check the lengths of pin pair group with Area DRC for the maximum and minimum wiring lengths.

## ● Electrical net maximum and minimum wiring length check

### [Function]

If you have set the maximum and minimum wiring lengths for electrical net as electrical net, you can check the lengths of electrical net with Area DRC for the maximum and minimum wiring lengths.

### Reference

For the electrical net, see "4-19 Electrical Net Operation."

## ● Confirmation dialog box for all area execution

### [Function]

With Rev. 5.0, you have to wait until the end of the process when you accidentally click [Check All Area].

Rev. 6.0 displays a confirmation dialog box when [Check All Area] is clicked.



## ● Interrupting Area DRC

### [Function]

With Rev. 5.0, you cannot interrupt a check once you start Area DRC.

With Rev. 6.0, you can interrupt a check.

This enables interruption of the process when you click [Check All Area] by mistake or set fault check items, so you do not have to wait until the process ends.

### [Operation]

Touch the following keys on the keyboard while Area DRC is being performed.

NT version: Ctrl+Break

HP version: Shift+Break

Solaris version: Shift+Break in the Kana mode if you are using the Japanese keyboard.

AltGraph+Shift+Break if you are using the English keyboard.

### [Notes and Restrictions]

- If you interrupt Area DRC performed for all areas, the status directly before interruption is left in the DRC history.
- While you can interrupt Area DRC, you cannot interrupt DRC recheck.
- Area DRC may not be interrupted immediately after the Break key is touched.

# 4-11 General DRC



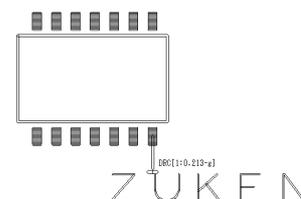
## [Function]

Rev. 6.0 supports a clearance check between a figure on a non-conductive layer and a figure on a conductive layer.

You can perform checks for figures between arbitrary non-conductive layers.

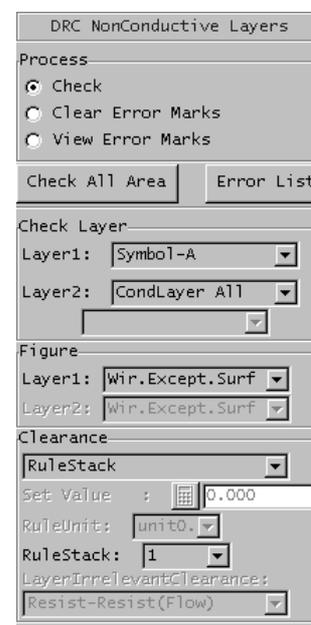
A check can be performed for the following combinations.

- Single non-conductive layer to all conductive layers
- Single non-conductive layer to single conductive layer
- Single non-conductive layer to non-conductive layer



## [Operation]

- (1) Select **DRC** → **DRC Non Conductive Layers** from the Placement/Wiring Tool menu bar.
- (2) Set [Check Layer] in the panel menu.  
Layer 1: Non-conductive layer to check  
Layer 2: Conductive or non-conductive layer to check
- (3) Set a clearance for the check.
- (4) Select an area to check by specifying the area or click [Check All Area].
- (5) If an error is detected, check error information with [Error List]. You can also check error information in the [View Error Marks] mode by clicking an error mark on the canvas.



## [Notes and Restrictions]

- A clearance check cannot be performed for intervals between conductive layers. To check this, use the Area DRC command.
- A clearance check cannot be performed for intervals between figures on a single non-conductive layer. (In other words, you cannot specify the same layer when setting the combination of non-conductive layers.)
- If you check intervals between non-conductive layers, you cannot select a rule stack while selecting a clearance.
- Error marks for clearance between non-conductive layers are always displayed regardless of the visible layer setting (ON/OFF) if [DRC error display] on the menu bar is set to ON.
- When a character is checked, the check is performed on the minimum rectangle enclosing the character.

# 4-12 Surface Slit Check

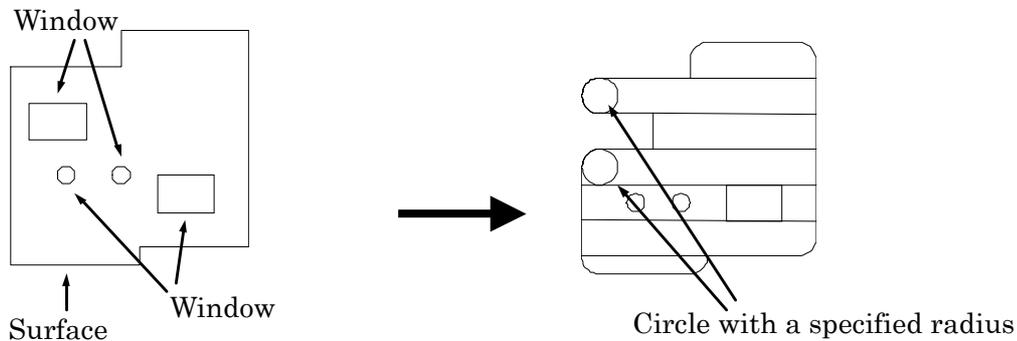


## [Function]

A function is added to check whether the conductive layer has a space where a circle with the radius specified with the surface pattern can be written.

This enables detection of a point where a filled area left in a surface is too large.

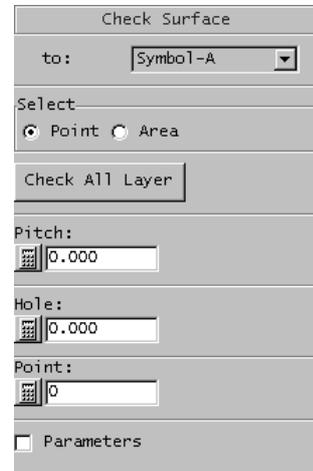
The point causing an error is output to the non-conductive layer specified as surface for the pen width specified on checking. You can easily modify the surface by using this surface as reference to create a slit. Because the hole in the padstack becomes a window on the surface, an error may be avoided by inputting a padstack. You can output a base position for padstack input.



## [Operation]

- (1) Select **Utility** → **Check Surface** from the menu bar.
- (2) Set a layer to which erroneous positions are output in [To:].
- (3) Set a radius for the circle to check.
- (4) Select a surface itself or by specifying the area and execute the Surface Slit check. Or click [Check All Layers] for execution.

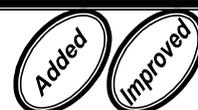
When the check is executed, erroneous points in the circle with the specified radius are output to a specified non-conductive layer.



## [Notes and Restrictions]

- This check targets surfaces and mesh planes. (A mesh plane is regarded as ordinary surface.)
- If the same shape as for check result surface exists on the output destination non-conductive layer, the surface is regarded as already checked and a check is not performed.
- If the set radius is 0, a check is not performed.

## 4-13 Query Function



The following functions are added or improved for each mode in the Rev. 6.0 Query command.

- Displaying placement limit and Component DRC group information in the “Component” mode
- Validating component surface specification in the “Pin” mode
- Displaying the shield attribute in the “Figure and area” mode
- Layers used to calculate padstack distance in the “Figure and area” mode changed
- Displaying the Wiring Keep-out attribute for padstacks in the “Figure and area” mode
- Displaying “Excluded” for the padstack non-conductive layer in the “Figure and area” mode
- Displaying clearance related to resist and symbol mark in the “Figure and area” mode
- Function to display distance to a PC board outline in the “Figure and area” mode
- Added information displayed related to test points in the “Figure and area” mode
- Function to individually display [Power supply] and [Ground] in the “Wiring status” mode
- Improved [Via Count] in the “Wiring status” mode
- Component comparison between PC board and CDB in the “Edited component” mode
- “Electrical net” mode

### ● Displaying placement limit and Component DRC group information in the “Component” mode

#### [Function]

With Rev. 6.0, you can define limits on the placement side and placement angle in the library and check the limits in the “Component” mode for the “Object info” function. Information on “Component DRC group” is displayed as well.

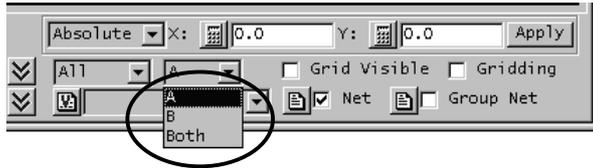
```
■■■ Component ■■■ (package symbol)
Reference           : C3
Coordinates        : [63.500,55.880]
Placement angle    : 270.000
Placement side     : B-side
Component symbol   : [Symbol-B] C3 (reference)
Stock code        : Z325A8039
:
:
Component group name : <undefined>
Component fixing phase : ANY_PHASE
Component fix status  : -
Attribute          :
Placement side limit : B-side (rule) B-side (CDB) B-side (soldering) B-side (package)
                   : B-side (conductive surface)
Angle permitted for placement : 0 90 180 (rule) 0 90 (CDB)
A-side height      :
B-side height     : 0.000 to 0.000
Component DRC group : 2014
User attribute     :
```

## ● Validating component surface specification in the “Pin” mode

### [Function]

If a component search layer is specified in the “Pin” mode for the “Object info” function, only component pins on the surface are selectable.

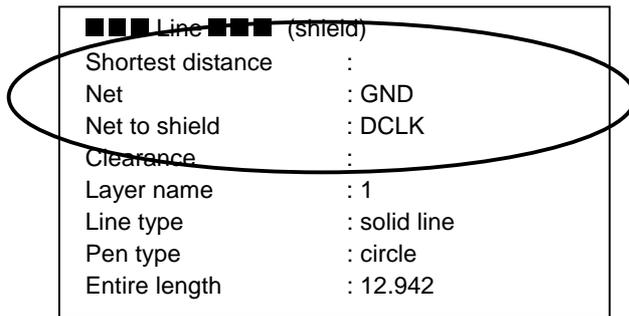
When “Component Search Layer” is set to “Both,” component pins on the A- and B-sides are selectable. When “A-side” is set, only components on the A-side are selectable and when “B-side” is set, only component pins on the B-side are selectable.



## ● Displaying the shield attribute in the “Figure and area” mode

### [Function]

When you refer to a shield pattern in the “Figure and area” mode for the “Object info” function, you can check the shield attribute and net name to shield.

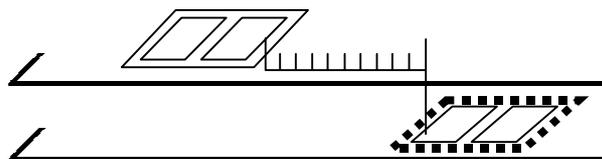


## ● Layers used to calculate padstack distance in the “Figure and area” mode changed

### [Function]

If the FROM layer of a padstack selected after is not between the FROM and TO layers on the padstack selected before when calculating the distance between padstacks in the “Figure and area” mode for the “Object Info” function, Rev. 6.0 displays the shortest distance between figures on each FROM layers.

This enables calculation of the distance between single layer padstacks of the A-side layer and B-side layer.



## ● Displaying the Wiring Keep-out attribute for padstacks in the “Figure and area” mode

### [Function]

With Rev. 6.0, you can add the Wiring Keep-out attribute for padstacks. “Wiring Keep-out” is displayed in the “Figure and area” mode for the “Object Info” function of the Query command.



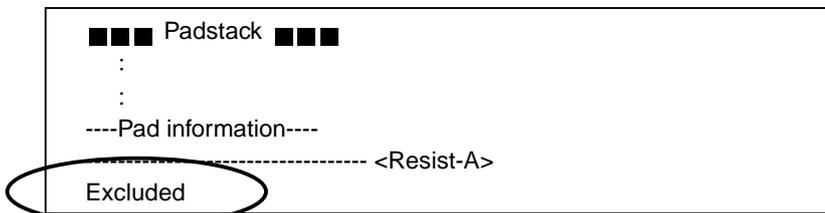
### Reference

For the padstack wiring keep-out attribute, see “4-17 Padstack Wiring Keep-out Attribute Support.”

## ● Displaying “Excluded” for the padstack non-conductive layer in the “Figure and area” mode

### [Function]

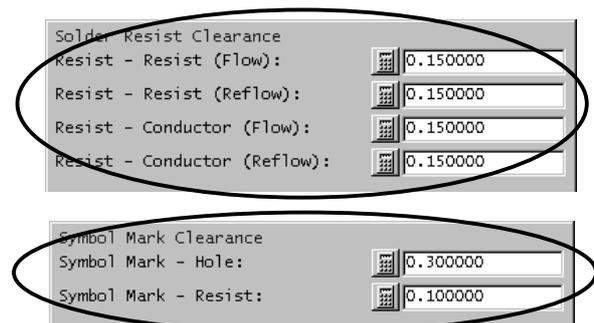
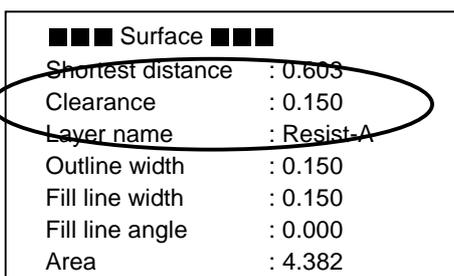
If a padstack has a figure on a non-conductive layer correlated to a conductive layer and the correlated conductive layer refers to a padstack not between the FROM to TO layers in the “Figure and area (detail)” mode for the “Object Info” function, “Excluded” is displayed at the point corresponding to the non-conductive layer.



## ● Displaying clearance related to resist and symbol mark in the “Figure and area” mode

### [Function]

If you select a figure on a resist or symbol mark layer in the “Figure and area” mode for the “Object info” function, Rev. 6.0 displays the corresponding “soldering resist clearance” and “symbol mark clearance” set as the design rule, “Clearance not related to the layer” in “Clearance:.”

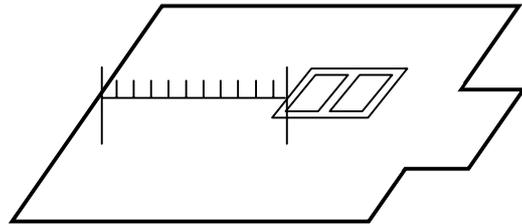


● **Function to display distance to a PC board outline in the “Figure and area” mode**

**[Function]**

When you select a PC board outline in the “Figure and area” mode for the “Object info” function, Rev. 6.0 displays the shortest distance between the outline and a figure selected immediately before (or after) in “Shortest distance:.”

■■■ Surface ■■■	
Shortest distance	: 2.700
Layer name	: PC board outline
Outline width	: 0.000
Fill line width	: 0.000
Fill line angle	: 0.000
Area	: 9156.566



● **Added information displayed related to test points in the “Figure and area” mode**

**[Function]**

When you refer to a figure with the test point attribute in the “Figure and area” mode for the “Object info” function, Rev. 6.0 displays “Reference name” and “Probe ID” in “Test point:.”

■■■ Padstack ■■■ (In-component)	
:	
:	
Test point: TP116 A-side	[128.230,20.320] PTP-2P2L

● **Function to individually display [Power supply] and [Ground] in the “Wiring status” mode**

**[Function]**

In the “Wiring status” mode for the “PCB Data” function, Rev. 6.0 displays power nets in “Power:” and ground nets in “Ground:.”

■■■ Wiring status ■■■				
	Net	Power	Ground	All
Number of nets	121	3	2	126
Number of pin pairs	207	105	138	450
Number of non-connected nets	0	0	0	0
Connection ratio	Net	: 100.000 %		
	Power	: 100.000 %		
	Ground	: 100.000 %		
	All	: 100.000 %		
Total wiring length	: 4619.984			
Number of Vias	: 159			

## ● Improved [Via Count] in the “Wiring status” mode

### [Function]

Rev. 6.0 does not count a single-layer padstack without a hole that is used as a test point or other for “Via count” in the “Wiring status” mode for the “PCB Data” function.

■■■ Wiring status ■■■				
	Net	Power	Ground	All
Number of nets	121	3	2	126
Number of pin pairs	207	105	138	450
Number of non-connected nets	0	0	0	0
Connection ratio	Net : 100.000 %	Power : 100.000 %	Ground : 100.000 %	All : 100.000 %
Total wiring length	: 4619.984			
Number of Vias	: 159			

## ● Component comparison between PC board and CDB in the “Edited component” mode

### [Function]

You can output information other than edited component information in the “Edited component” mode for the “PCB Data” function.

- Compares user versions of PCB and CDB objects and outputs different ones.
- Compares footprints referred to by a component in the PCB and footprints related to the parts in the CDB and outputs different ones.

### [Notes and Restrictions]

- You must set board.rsc.

### Reference

To set board.rsc, see “1-4 List of Changed Resource Files ●\$ZUEROOT/info/board.rsc.”

## ● “Electrical net” mode

The “Electrical net” mode is added for the Query command as the electrical net is supported.

- Electrical net reference
- Specifying a net in the Set Net Display Color dialog box

### Electrical net reference

#### [Function]

Rev. 6.0 outputs information on electrical nets to the Query command during electrical net operation.

If the electrical net name, net names making up the electrical net, the number of pin pairs, the number of non-connected nets, the total wiring length, the number of Via are set, information on these rules and on the maximum and minimum wiring lengths is output.

#### [Notes and Restrictions]

- For electrical net operation, set “useENet” to “On” in the resource file, board.rsc.

### Specifying a net in the Set Net Display Color dialog box

#### [Function]

When you execute the Query command for an “electrical net,” double-clicking a net name in the Net Display Color dialog box displays information on the electrical net made up of the net in the Query window.

#### [Notes and Restrictions]

- If the double-clicked net does not make up an electrical net, the net is regarded as one electrical net and related information is output.
- For electrical net operation, set “useENet” to “On” in the resource file, board.rsc.

#### Reference

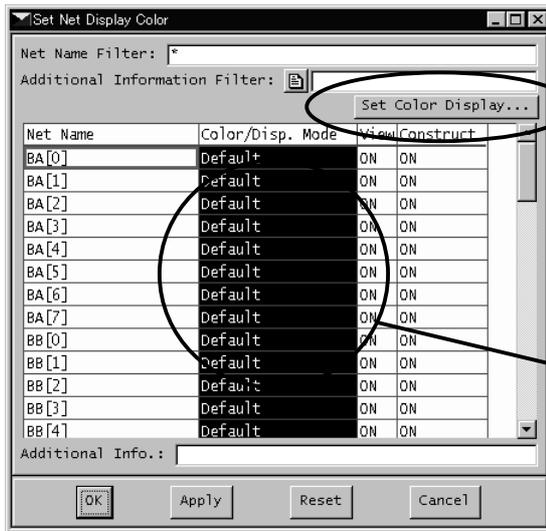
For the electrical net, see “4-19 Electrical Net Operation.”

# 4-14 Set Net Display Color Dialog Box



The following functions are added for the Set Net Display Color dialog box.

- Color setting per object
- Display mode setting
- Deleted lock attribute item



Color setting per object

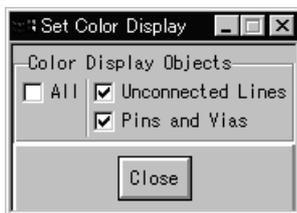
Display mode setting

## ● Color setting per object

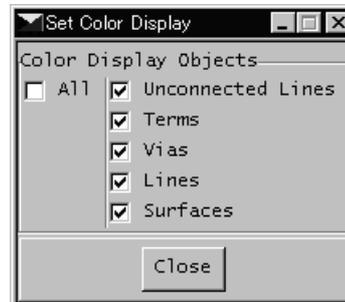
### [Function]

You can specify an object for which a net display color is set in detail.

**Rev.5.0**



**Rev.6.0**



### [Notes and Restrictions]

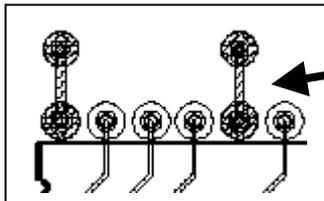
- Display color for pads refers to the Via setting.

## ● Display mode setting

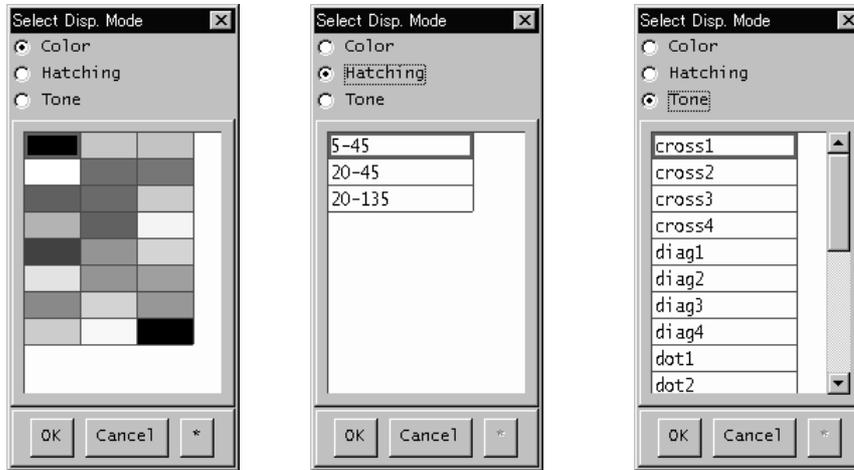
### [Function]

According to the Rev. 5.0 net display color setting, the same color is set to all nets, so you cannot see to which layer data belongs.

With Rev. 6.0, you can set the “display mode” (hatching and tone pattern) in addition to the conventional color setting. This enables easy recognition of overlapping objects.



While the color setting for the layer is maintained, the display mode for a specific net is changed.



Set hatching and tone pattern in the resource file, board.rsc. (They are referred to at tool activation.)

#### board.rsc

Hatching	Creates a table for hatching (index, hatching name, interval, angle). <pre>hatchTable 4 {   1 "5- 45"      5      45   2 "20- 45"    20     45   3 "20- 135"   20    135 }</pre>
Tone	Specify a bit-map filename in the table for tone. (This is already available with Rev. 5.0.) <pre>toneTable 2 {   1 cross1.xbm   2 cross2.xbm   3 cross3.xbm   4 cross4.xbm }</pre>

## [Notes and Restrictions]

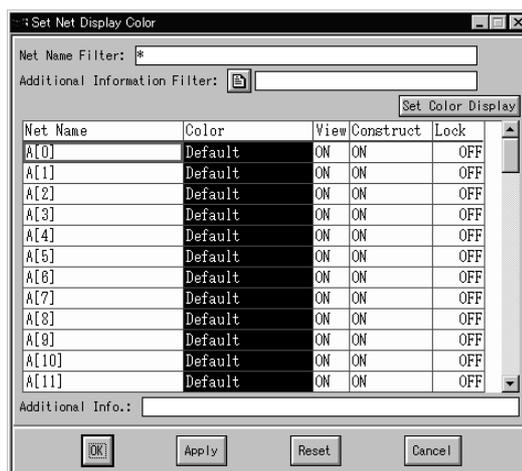
- The net display setting has priority over the display setting specified with the layer attribute. Therefore, if the layer attribute specifies display without width and the display mode is set as net display, tone with width or hatching display is employed.
- You cannot change the net display color and display mode at the same time. When the display color is changed, the display mode is that specified by the layer attribute. When the display mode is changed, the display color is that specified by the layer attribute.
- While you can port the net display color set on the SD to BD, you cannot port or import the display mode to or from the SD.
- Although the Print command supports the net display mode, tone is displayed with width under some Print command specifications.

## ● Deleted lock attribute item

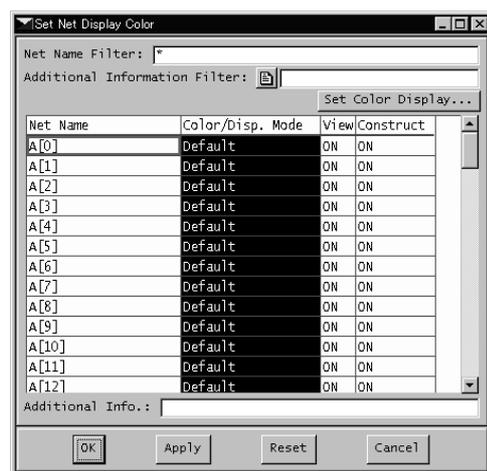
### [Function]

The Rev. 5.0 Set Net Display Color dialog box had the “lock attribute” column which was used only by automatic wiring tools (Route Editor or SPECCTRA). This column has been deleted in Rev. 6.0 because the “wiring object lock attribute” set with **Attribute** → **Wire Lock** on the menu bar is referred to.

Rev.5.0



Rev.6.0



## [Notes and Restrictions]

- If the “net lock attribute” is set to ON for objects on Rev. 5.0 or older, set the “wiring object lock” for such objects before automatic wiring.

# 4-15 Improved Display Function



The following functions are added or improved for display.

- Cursor Information dialog box
- Display command for panel data
- Improved grid display function
- Function added to display component reference points
- Improved display for overflow caused by enlargement or reduction
- Changed marker size
- Resourcing of negative figure display mode for display with width is made resource

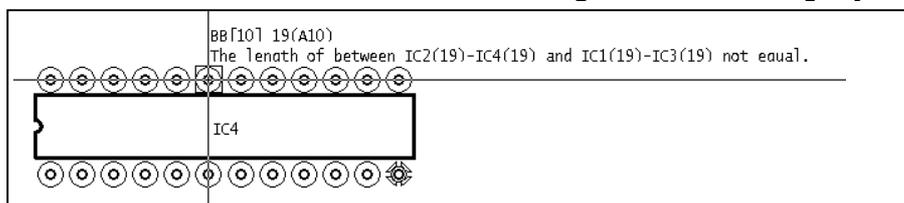
## ● Cursor Information dialog box

### [Function]

Although reference, net name and many other types of information can be displayed as cursor information, this much information sometimes obstructs operation.

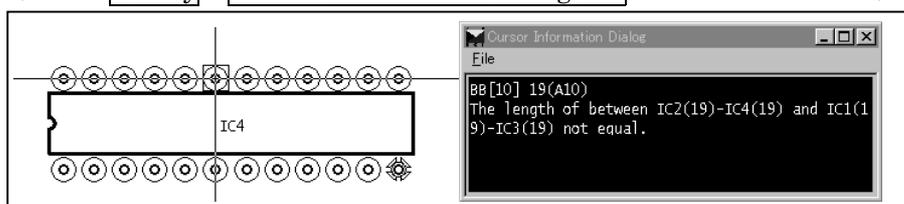
To avoid this inconvenience, Rev. 6.0 has the Cursor Information dialog box, which enables display of information in a different window.

#### <When the Cursor Information dialog box is not displayed>



#### <When the Cursor Information dialog box is displayed>

(Select **Utility** → **Cursor Information dialog box** from the menu bar)



### [Notes and Restrictions]

- The Cursor Information dialog box only displays information selected in “Cursor information” in the Assist Menu.
- During Cursor Information dialog box display, nothing is displayed at the cursor.
- The pin wiring order number is not displayed in the Cursor Information dialog box.
- [Display Design Information] can be displayed only if you have Quick User Rule Verifier (optional).
- [Topology information display] is displayed only with the Cursor Information dialog box.
- [Display Analysis Results] and [Marking] are not displayed with the Cursor Information dialog box.

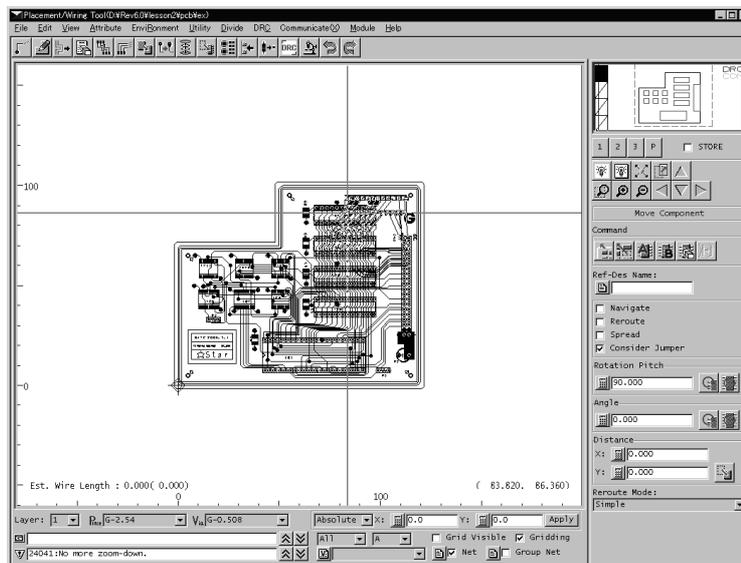
## ● Display command for panel data

### [Function]

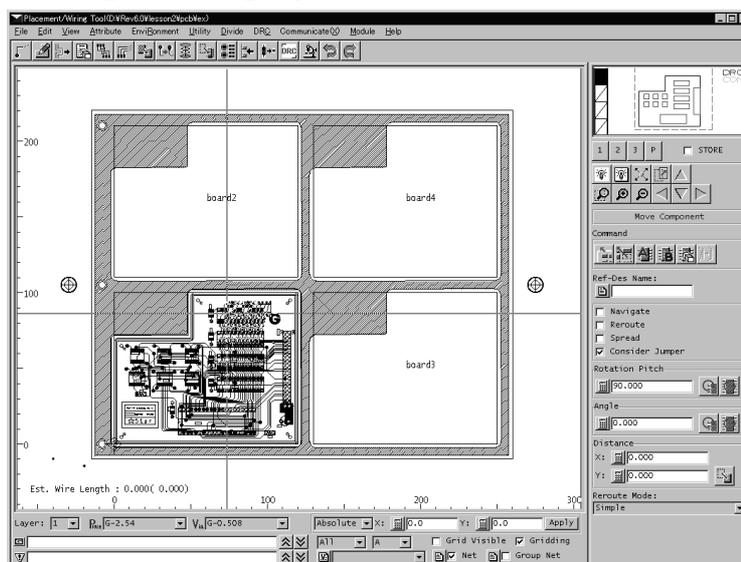
With Rev. 5.0, after you input a sub-PC board with the Panel Tool, you have to edit the sub-PC board itself.

With Rev. 6.0, you can edit a sub-PC board by referring to the panel data display and editing data on the PC board. Supporting tools include the Placement/wiring, Floor Plan, Artwork and PC Board Outline Edit Tools. This enables editing of a sub-PC board by checking data on the panel.

### <Without panel display>



### <With panel display>



### [Notes and Restrictions]

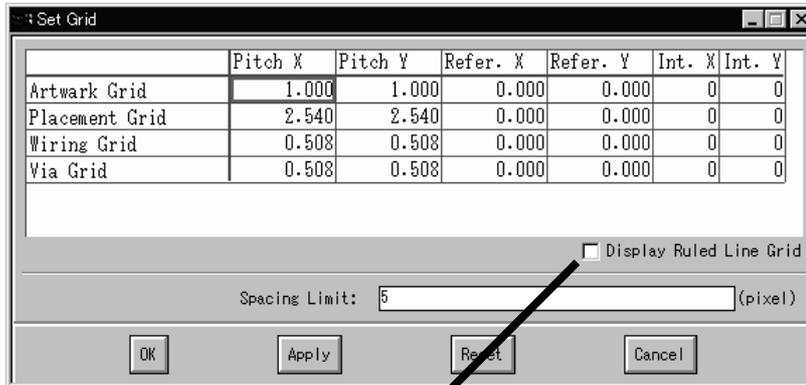
- Data on panels are for display only and cannot be edited.

## ● Improved grid display function

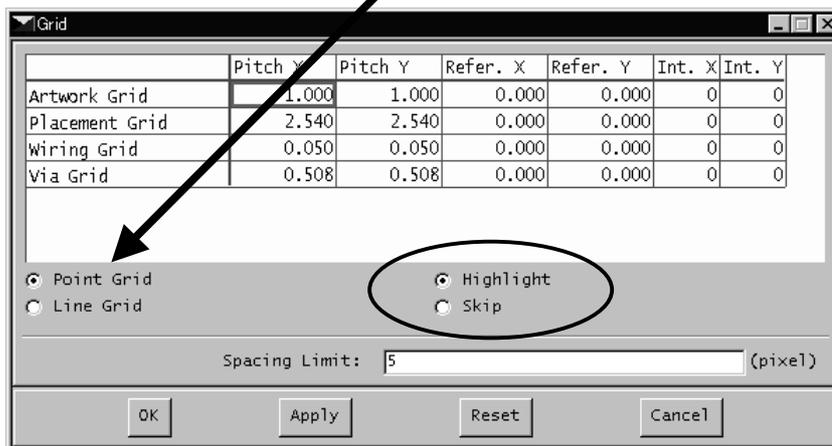
### [Function]

Operability and terms are in line with CDB. This function supports the skip display mode in addition to the conventional highlight display mode.

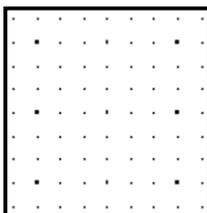
#### Rev.5.0



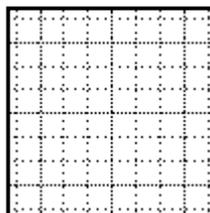
#### Rev.6.0



#### Highlight display

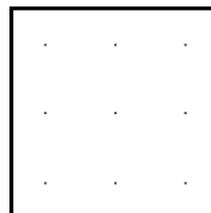


Point grid

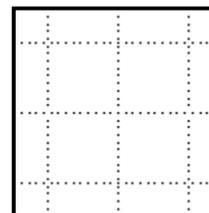


Line grid

#### Skip display



Point grid



Line grid

## ● Function added to display component reference points

### [Function]

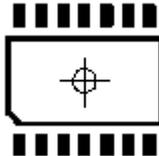
Rev. 6.0 has a new function to display a mark at the component reference point.

This function is available with the Board Designer and Board Producer.

You can select a component placement side to display from, **Both**, **A-side** and **B-side**.

### [Operation]

Select **View** → **Component Origin** → **On** from the menu bar.



## ● Improved display for overflow caused by enlargement or reduction

### [Function]

With Rev. 5.0, when enlargement or reduction is performed with area zoom or other tools and the specified enlargement (reduction) ratio exceeds the display limit, the error message, “Cannot zoom in (out) more.” appears and the display area remains unchanged.

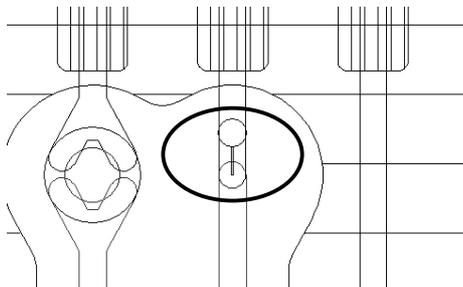
When the specified enlargement (reduction) ratio exceeds the limit, in Rev. 6.0, the area is enlarged or reduced as much as possible and the error message is displayed.

This enables easy understanding of the display limit.

## ● Changed marker size

### [Function]

The sizes (pixels) of ‘+,’ circle and flag marks have been enlarged and are now easier to see.



### Reference

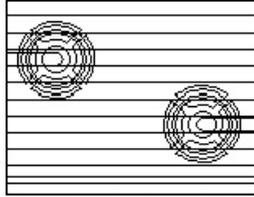
For the marker size setting, see “1-4 List of Changed Resource Files  
●\$ZUEROOT/info/board.rsc.”

● Resourcing of negative figure display mode for display with width is made resource

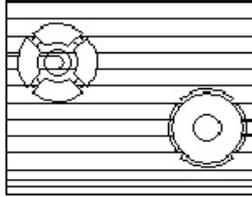
[Function]

Rev. 5.0 was changed so that negative figures (hole, thermal, land and clearance lands) are blackened if the layer display attribute is “with width.” With Rev. 6.0, you can set whether to blacken such figures in the resource file.

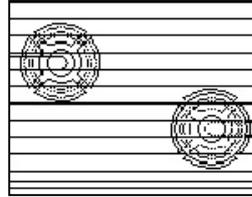
<none>



<solid>



<tone>



The following keywords are added to board.rsc.

Keyword	Default	Description
clrLndDrawMode	none	none : Only displays outlines. solid : Blackens the inside of the outline. tone : Draws a black tone pattern in the inside of the outline.

---

# 4-16 Padstack Plating Attribute Support

---



With Rev. 5.0, the padstack with Plating Attribute “No” (hereafter, Via without plating) is treated the same as the Via with Plating Attribute “Yes.” Rev. 6.0 regards Vias without plating as non-conductive for processing.

- Automatically changing the land status
- Net connection calculation
- Extraction and retraction on input
- DRC

## [Notes and Restrictions]

- There are no changes for padstack processing with 3rd vendor tools. Vias without plating are processed the same as ordinary Vias.

## Reference

For details on handling the padstack plating attribute, see “Board Layout System/Board Designer User’s Guide, Vol.2, Interactive Design/4.9 Treatment of Padstack Plating attribute.”

## ● Automatically changing the land status

### [Function]

The BD has a built-in function to automatically change land status in order to optimize it for the current padstack and conductor connection.

With Rev. 6.0, Vias without plating are not connected when land status is automatically changed.

## ● Net connection calculation

### [Function]

The BD has a built-in function to calculate net connection status by using overlapping of conductive figures.

If a Via without plating overlaps a conductive figure, Rev. 6.0 sees it as “there is no net connection” and outputs non-connected nets.

## [Notes and Restrictions]

- If a pattern is connected on the uppermost and lowermost layers of the Build-up Via without plating shown below, net connection is maintained.
  - “Build-up Via”: ON
  - Inner layer connected land is not registered.

## ● Extraction and retraction on input

### [Function]

Wire Input command: the system has been improved so that extraction and retraction cannot be normally performed for Via without plating when you extract or retain a line to/from a padstack.

### [Notes and Restrictions]

- The automatic wiring tool and other tools do not consider plating attribute on extraction and retraction. Vias without plating are processed the same as ordinary Vias.

## ● DRC

### [Function]

Area DRC command has been improved to issue an error if a Via without plating is connected.

---

# 4-17 Padstack Wiring Keep-out Attribute Support

---



## [Function]

With Rev. 6.0, you can set the Wiring Keep-out attribute to padstacks.

A padstack with Property “noWiring” set to “YES” in CDB is regarded as a wiring keep-out padstack.

This attribute is valid when the padstack is used for installation hole or other purposes.

Processing for padstacks with the wiring keep-out attribute is listed in the table below.

### <Function supporting padstacks with the wiring keep-out attribute>

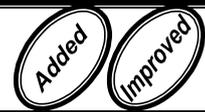
Function/command	Processing
Area DRC/DRC recheck	If a padstack with the wiring keep-out attribute touches the conductor for line or surface with a net, a short error occurs.
Wire Input	Extraction and retraction are not performed for a padstack with the wiring keep-out attribute. When a padstack with the wiring keep-out attribute is input as Via, retraction to other figures is not performed.
Surface input	A padstack with the wiring keep-out attribute is regarded as an inhibited figure. A surface is cut out at the point where the surface overlaps a padstack.
Logical net editing	If nets are set to directly be allocated during net connection, a net is not allocated to a padstack with the wiring keep-out attribute.
Check/net building during net connection	A net is not allocated to a padstack with the wiring keep-out attribute. Even if a surface or line with net is connected to a padstack with the wiring keep-out attribute, a net is not allocated.
Pattern Connection Pin List Output Program (bdnetout)	This program does not refer to the wiring keep-out attribute for padstack. If the wiring keep-out attribute is set to a padstack, it is regarded as an ordinary padstack.

## [Notes and Restrictions]

- When Padstack Property “noWiring” is set to a character string other than “YES,” the padstack is regarded as having the “wiring keep-out” attribute.

To clear this attribute, delete “YES” from “noWiring” to reset.

# 4-18 Improved Operability



The following functions are added or improved.

- Information menu design change
- Added grid change list function
- Function added to display comments for the active layer
- List for switching visible layer groups
- Menu to specify coordinates
- Function to add land status normalization mark
- Improved active layer data selection operation

## ● Information menu design change

Design of the information menu has been changed to improve operability.

- Artwork (PC Board Outline) Tool



- Placement/Wiring Tool



- Floor Plan Tool



Rev. 5.0 redisplay the screen when another tool is selected as the canvas size changes. In contrast, the information menu size is unified for all Rev. 6.0 tools so that you can seamlessly move between tools.

## ● Added grid change list function

### [Function]

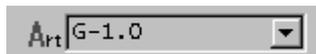
When you have set a grid in the Grid Set dialog box on Rev. 5.0, you cannot check the grid once you have closed the dialog box.

The Rev. 6.0 information menu grid setting allows easy changing or checking of the grid.

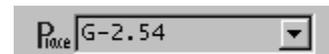
#### • Placement/Wiring Tool



#### • Artwork (PC board Outline Edit) Tool



#### • Floor Plan Tool



### [Notes and Restrictions]

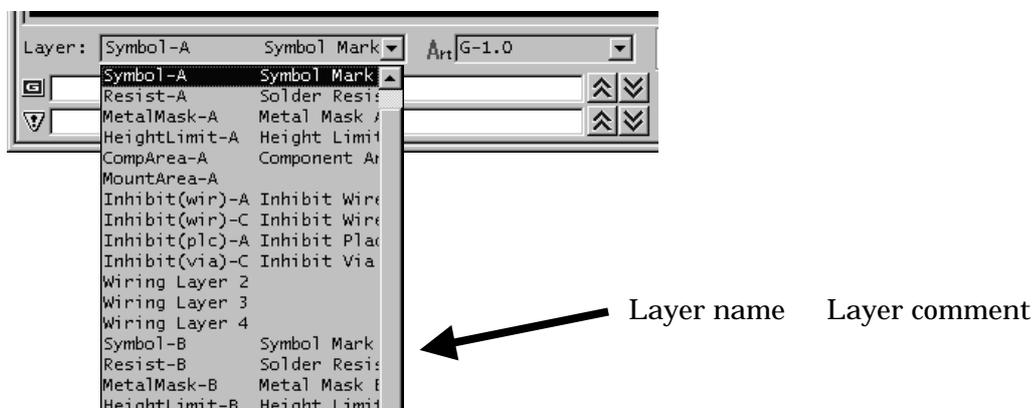
- This function does not support switching the line/point grids, switching the highlight display/skip display and changing an interval.
- This function does not support a temporary grid setting.

## ● Function added to display comments for the active layer

### [Function]

If a layer comment is set on Rev. 5.0, you cannot check it without using the Visible Layer Setting dialog box or others.

The Rev. 6.0 Artwork Tool displays comments in the Active Layer pull-down menu.



### [Notes and Restrictions]

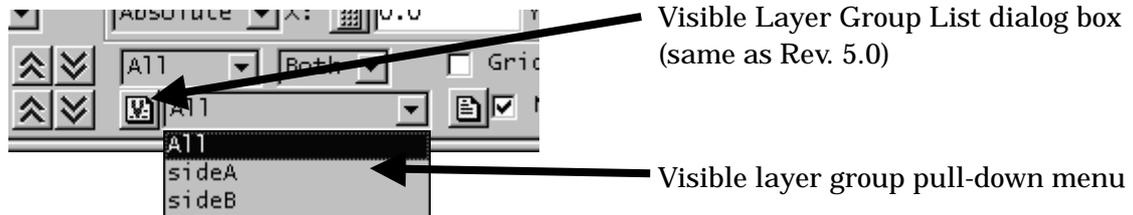
- The Placement/Wiring Tool and Floor Plan Tool do not support this display function.

## ● List for switching visible layer groups

### [Function]

Because you can set visible layer groups only with the dialog box on Rev. 5.0, you cannot check them once you closed the dialog box.

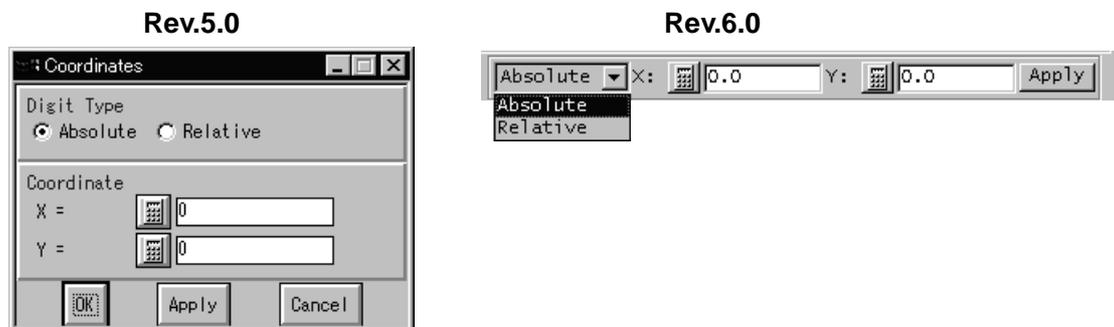
To avoid this inconvenience and improve visibility, Rev. 6.0 has the pull-down menu. You can set a visible layer group with the box.



## ● Menu to specify coordinates

### [Function]

While the “Coordinates” dialog box is used to specify coordinates on Rev. 5.0, the Rev. 6.0 information menu has the item for inputting coordinates. Therefore, you do not have to open the Coordinates dialog box.



### [Notes and Restrictions]

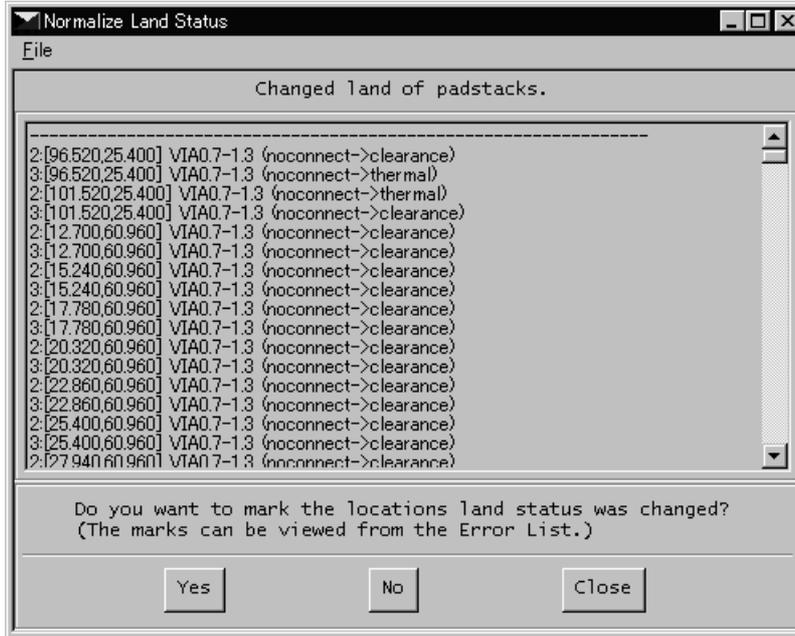
- You can also use the Coordinates dialog box on Rev. 6.0.

## ● Function to add land status normalization mark

### [Function]

The BD has a built-in function to automatically change land status in order to optimize it for the current padstack and conductor connection.

Rev. 6.0 adds a mark to the changed position, enabling location of changed positions (which layer in which padstack is changed.)



## ● Improved active layer data selection operation

### [Function]

If the visible layer setting for the active layer is not activated and [Display]→[Active Layer Display] is cleared (that is, the active layer is not displayed), data on the active layer is not searched.

### [Notes and Restrictions]

- If [Single layer] is selected, there is no search target.

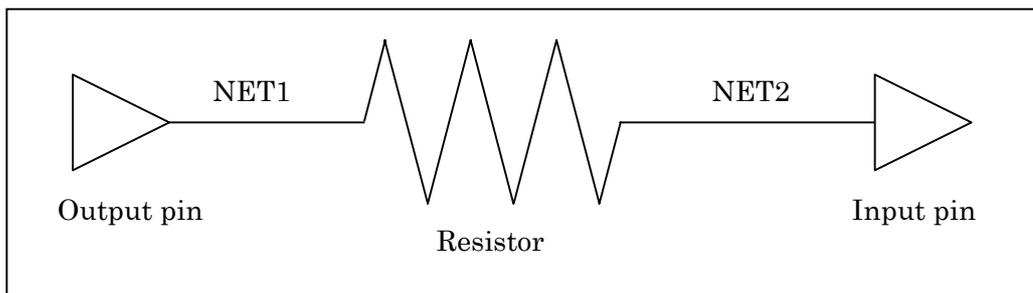
# 4-19 Electrical Net Operation



## [Function]

The electrical net (hereafter, E-net) is a group of nets regarded as one unit in terms of signal flow during digital schematic design.

“NET1” and “NET2” in the figure below are regarded as separate nets on the BD because the potentials are different. However, they process the same digital signal. A group of nets where “the same digital signal flows” is considered to be “E-net” on the BD.



## Preparations

### Tool resource file setting

If you operate E-nets on the BD, preset the tool resource file, “board.rsc.”

UseENet : On

### Component library registration

You can add attributes to control E-nets for the component pin and part as needed.

Component pin/gate function pin attribute: enetSeries  
Part attribute: enetNonSeries

## Schematic design

### Net input

Create an E-net with the SD Electric Net Editor.

## PC board design

### PC board generation

Generate a PC board as an ordinary PC board.

### Design rule setting

Using the Design Rule Editing Tool for the PC board, you can set the E-net maximum and minimum wiring lengths and batch-edit the attributes of nets making up the E-net.

## Reference

To set design rules, see “3-3 Design Rule Editing Tool • Setting new rules.”

— Query command —

Using this command, you can display information on the E-net.

 Reference

For the Query command, see “4-13 reference function •“electrical net.””

— Area DRC —

When “Maximum and minimum wiring lengths” is set to ON, the “maximum and minimum wiring lengths” of E-net are checked as well.

— Transmission Line Analysis command —

The Transmission Line Analysis command refers to E-nets.

— E-net rebuilding —

Reflecting changes in the net during PC board design, you can rebuild E-net according to the same rules as the SD. Rebuild E-net to reflect attributes set to components and pins on the CDB afterward to E-net definition or to define E-net for PC board data created on Rev. 5.0 or older.

 Reference

For electrical net operation, see “Board Layout System/Board Designer User’s Guide, Vol.2, Interactive Design/Chapter 21 E-net Operation.”

**[Notes and Restrictions]**

- E-net-supporting commands are valid only when “useENet” is set to “On” in the resource file, board.rsc.
- If you set pin and component attributes on the SD schematic and transfer them to the BD with “Board Generation” or “Forward Annotation,” and then set different values for the attributes in the CDB, the attributes set on the SD have priority in the Rebuild Electrical Net command for the BD.

For example, presume that you set “Yes” to Attribute “enetNonSeries” for a component on the SD and you reset “No” to Attribute “Electrical Net Non Series” for the same component in the CDB. In this case, “Yes” has priority.

---

# 4-20 Design of Inner-layer Component

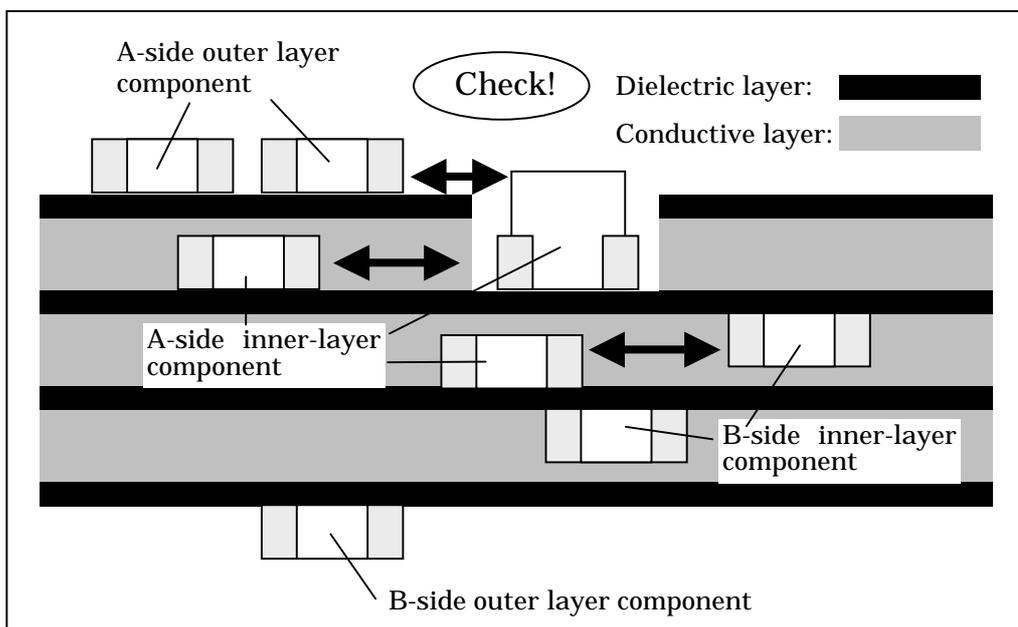
---



## [Function]

By using technology layer mapping, you can design inner-layer components on the BD. However, because Rev. 5.0 does not have a check function, you have to visually check the design, making a mistake highly likely.

With Rev. 6.0, the component attribute has a layer number so that you can design or check presuming an actual PC board.



The following checks are performed.

- Scaling check for components on the inner layer (the same layer)
- Scaling check with a component on another layer considering the foil and dielectric thicknesses
- Wiring keep-out check for a layer other than a foil-printed surface

## Preparation

### Footprint registration

Register a footprint for the inner layer. Set a footprint attribute (Attribute name: placeLayerNo, attribute value: inner layer number) to identify the inner layer. Component areas are input in the same surface layer.

### Technology creation

Perform layer mapping so that the registered footprint shapes are mapped onto the inner layer.

### Design rule setting

Set the foil and dielectric layer thicknesses for each layer. This setting is referred to with the component height during component placement design and used for the interstitial component scaling check (Component DRC).

## PC board design

### PC board generation

Generate a PC board as an ordinary PC board.

### Conductive surface setting

Set which inner layer side the foil is printed on during production to avoid placement on the side that is not the conductive surface. Set the conductive surface with the cmpset program (- m condside).

### Setting components to the inner layer

To set components to the inner layer, use [Footprint Change] for the "component change" command. You can handle them as the A- or B-side component, the same as outer layer components after setting.

### Component DRC

A check is performed considering inner-layer components during placement-side limit check and component overlap check.

## Reference

For inner-layer component design operations, see "Board Layout System/Board Designer User's Guide, Vol.1, Design Preparation/Chapter 12 Design and Operation of Inner-layer Component."

## [Notes and Restrictions]

- Wiring keep-out areas are handled as the wiring keep-out area for all layers.
- A height limit area is defined only for the outer layer.
- The following checks cannot be performed.
  - Resist missing check for inner layers
  - Missing check related to metal mask
  - Annular-ring check (MRC)
- If a hole exists in the padstack in the footprint for inner-layer components, you cannot represent components as interstitial pins.
- Specify "0" or "a number between 2 and the number of layers minus 1" for the "inner layer number" set as the footprint attribute. A component with Inner layer Number 0 is not checked by the component area check or conductive surface check. (This is used for a printed component with a pin.)

---

# 4-21 Component List Output Program (bdplist)

---



The following output items are added for the Component List Output Program (bdplist).

- The mode setting `-180 - 180` to a component angle
- Mirroring function (X or Y)
- Rotation function
- Scale function
- Offset function
- Outputting X- or Y-coordinate for the component
- Outputting the component height, `From_To`
- Outputting component symbol information
- Outputting whether a footprint is dedicated
- Outputting footprint technology
- Sorting in group

You can specify these added items by using each optional parameter or specifying it in the Edit Format Definition File (EDF).

```
bdplist.sh -r PCB database name
           -p edit   Format filename   [Optional parameter]
```

**\* On the Windows-version, use `bdplist.exe` for activation.**

- With an optional parameter  
Specify an optional parameter in [Optional parameter] of the above starting statement.
- With the edit format  
Write the items in the “edit format definition file (EDF)” prepared upon activation.

Example of an Edit Format File (EDF)

```
unit      (millimeters)
delimiter (" " "\ n")
separator ("| " ",")
outputDir ("./")
outputFile ($pcbPath ".plf")
width     (0)
continue  (" ")
outputFormat {
    (Comp      reference)
    (Comp      originalId)
}
```

You can specify both for certain items. If there are two specifications, specification with the optional parameter has priority.

## ● The mode setting $-180 - 180$ to a component angle

### [Function]

Although you can only set a value between  $0^\circ$  and  $360^\circ$  to a component angle on Rev. 5.0 or older, a new mode to output data between  $-180^\circ$  to  $180^\circ$  is added for Rev. 6.0.

### [Operation]

- Specifying an optional parameter

**-p: maxAngle angle**

- Specifying with the edit format

**maxAngle (angle)**

Specify 180 or 360 in angle. (Default: 360)

180:  $-180 \leq \text{angle} \leq 180$

360:  $0 \leq \text{angle} \leq 360$

## ● Mirroring function (X or Y)

### [Function]

A mode is added to output coordinate and angle information after X- or Y- coordinate reversion.

### [Operation]

- Specifying an optional parameter

**-p: mirror mirror mode**

- Specifying with the edit format

**mirror {mirror mode}**

Specify X, Y or OFF in mirror mode. (Default: OFF)

X: X-coordinate reversion

Y: Y-coordinate reversion

OFF: No reversion

## ● Rotation function

### [Function]

A function is added to output coordinate and angle information after rotating the PC board by the specified angle using the origin (0, 0) as center.

### [Operation]

- Specifying an optional parameter

**-p: rotate rotation angle**

- Specifying with the edit format

**rotate (rotation angle)**

Rotation angle: specify a real number within the range  $0 \leq \text{value} < 360$ . (Default: 0)

## ● Scale function

### [Function]

A function is added to output coordinate information after being scaled by the specified value.

### [Operation]

- Specifying an optional parameter

**-p: scale scale value**

- Specifying with the edit format

**scale (scale value)**

Scale value: specify a real number larger than 0. (Default: 1)

## ● Offset function

### [Function]

A function is added to output coordinate information after offset by the specified value.

### [Operation]

- Specifying an optional parameter

**-p: offset offset value X, offset value Y**

- Specifying with the edit format

**scale (offset value X offset value Y)**

Specify real numbers for both offset values. (Default: 0,0)

The following characters are used to delimit the offset value X and Y.

- For the optional parameter, comma
- For the edit format, space

### [Notes and Restrictions]

- Coordinate and angle conversions (mirror, rotation, scale and offset) are executed in the following order if some of them are specified at the same time.

Mirror → rotation → scale → offset

## ● Outputting X- or Y-coordinate for the component

### [Function]

Although X- and Y-coordinates are set for display on Rev. 5.0, for example, 0.000, 0.000, Rev. 6.0 enables output of one of them.

### [Operation]

- Specifying with the edit format

Class	Item	Output value
Comp	CoordX	X-coordinate for component
	CoordY	Y-coordinate for component
	insideCoordX	X-coordinate for component on the PC board
	insideCoordY	Y-coordinate for component on the PC board
	outsideCoordX	X-coordinate for component outside of the PC board
	outsideCoordY	Y-coordinate for component outside of the PC board

(A value is output in the form of real number; precision is referred to for digits below the decimal point.)

### [Notes and Restrictions]

- You can also use Coord (component coordinates X, Y) that was used on Rev. 5.0.

## ● Outputting the component height, From\_To

### [Function]

With Rev. 6.0, you can output component height information (From\_To). The height information refers to part, package and footprint information and is determined from their maximum and minimum values.

### [Operation]

- Specifying with the edit format

Class	Item	Output value
Comp	heightFrom	Placement side component height From (minimum height)
	heightFromA	A-side component height From (minimum height)
	heightFromB	B-side component height From (minimum height)
	heightTo	Placement side component height To (maximum height)
	heightToA	A-side component height To (maximum height)
	heightToB	B-side component height To (maximum height)

(A value is output in the form of real number; precision is referred to for digits below the decimal point.)

## ● Outputting component symbol information

### [Function]

With Rev. 6.0, you can output a character string and coordinates for component symbols. After specifying a non-conductive layer name, output information on the component symbol on the layer.

### [Operation]

- Specifying with the edit format

Class	Item	Output value
Comp	non-conductive layer name	Character string for the component symbol on the specified layer
	non-conductive layer name	X- and Y-coordinates for the component symbol on the specified layer

(A value is output in the form of real number; precision is referred to for digits below the decimal point.)

### [Notes and Restrictions]

- If the same layer contains multiple component symbols, information on only one symbol is output.

## ● Outputting whether a footprint is dedicated

### [Function]

With Rev. 6.0, you can output footprint information indicating whether the footprint is a dedicated footprint.

### [Operation]

- Specifying with the edit format

Class	Item	Output value
FootPrint	private	PRIVATE (dedicated) or NotPRIVATE (common)

## ● Outputting footprint technology

### [Function]

A mode is added to output technology names as footprint information.

You can output technology names for all components in one mode and technology names for components using technologies other than default in another mode.

### [Operation]

- Specifying with the edit format

Class	Item	Output value
FootPrint	technology	Technology name (output for all)
	otherTech	If a technology is other than default, technology names are output. If a technology is default, default character strings are output.

## ● Sorting in group

### [Function]

A function is added to sort grouped items.

For example, if you group references by part names and output the group, you cannot sort references displayed in the group again on Rev. 5.0 or older.

With Rev. 6.0, you can sort them by another key in such a case.

#### Rev. 5.0

0.33uF	: C81,C96,C4	: CHIP2014
SN74LS08	: IC32,IC2	: SOP14

#### Rev. 6.0

0.33uF	: C4,C81,C96	: CHIP2014
SN74LS08	: IC2,IC32	: SOP14

### [Operation]

- Specifying with the edit format

#### Example of edit format

```
outputFormat {  
  (Part      group      up      alnum)  
  (Comp     reference  up     alnum)  
  (Footprint name      )  
}
```

### [Notes and Restrictions]

- Only one sorting key is used for references in a group. Items other than one first found are ignored.

## 4-22 Other improvements



The following functions are added or improved for Rev. 6.0.

- Moving the PC board origin
- Added function for the Pattern Connection Pin List Output Program
- Supporting cross-probing for multiple nets

### ● Moving the PC board origin

#### [Function]

The origin move mode is added for the Component Information Input/Output Program (cmpset). This enables the movement of the origin for PC board data (PCB) and panel data (PNL).

#### **-m moveorg**

Origin move mode.

#### **-p: x move in the X-direction**

Specify the X-coordinate to which the origin is moved.

\* When this is omitted, the default is 0.

#### **-p: y move in the Y-direction**

Specify the Y-coordinate to which the origin is moved.

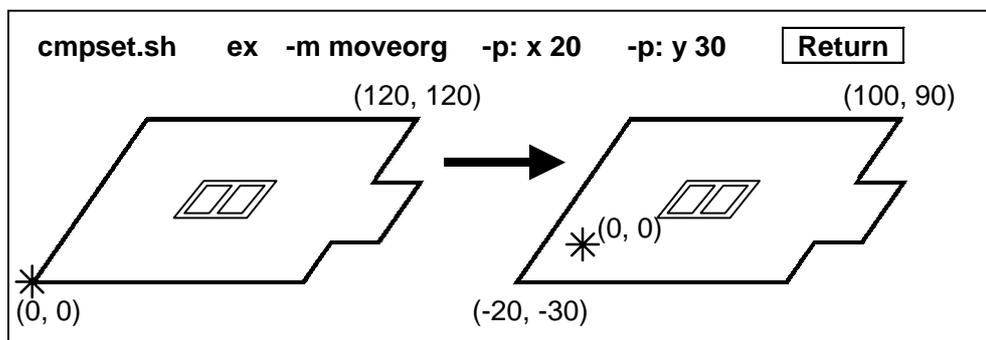
\* When this is omitted, the default is 0.

#### **-m coordinates**

Specify a unit in specifying coordinates from [mm/inch/mil/micron].

\* If this is omitted, the default is mm.

<Example> The origin in the PCB file “ex” is moved to (20, 30).



#### Reference

This Reference Manual on New Software Functions covers only optional parameters added to Rev. 6.0.

For details on cmpset, see the User's Guide.

## ● Added function for the Pattern Connection Pin List Output Program

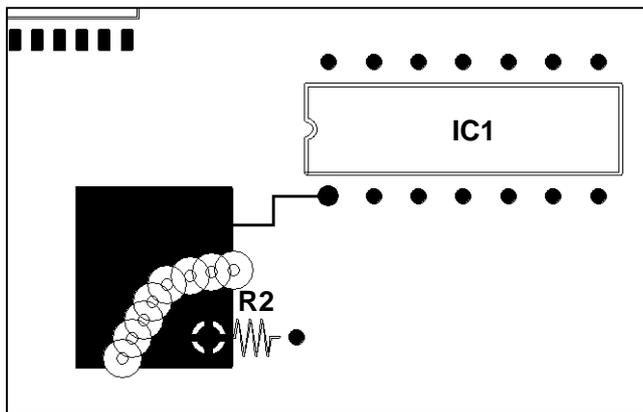
### [Function]

Rev. 5.0 outputs a pin connected to the same surface divided by a clearance land or thermal land as shown in the figure below to the net list as the same net.

With Rev. 6.0, you can output them as different nets by specifying an option (- m detail). A pattern connected via padstack without plating is regarded as non-connected net and output as different net.

**b d netout.sh -m detail Required parameter**

\* On the Windows-version, use **bdnetout.exe** for activation.



**(Rev.5.0)**

```
DT000001 : : SN74LS08-DIP : AND2 : IC1 : 1 : : 1.cmp1 : 1A : PACKAGESYMBOL ;
DT000001 : : 330OHM : : R2 : 1 : : 1.cmp20: T1 : PACKAGESYMBOL ;
: : SN74LS08-DIP : AND2 : IC1 : 2 : : 1.cmp : 1B : PACKAGESYMBOL ;
: : SN74LS08-DIP : AND2 : IC : 3 : : 1.cmp1 : 1Y : PACKAGESYMBOL ;
```

**(Rev.6.0)**

```
DT000001 : : SN74LS08-DIP : AND2 : IC1 : 1 : : 1.cmp1 : 1A : PACKAGESYMBOL ;
DT000002 : : 330OHM : : R2 : 1 : : 1.cmp20: T1 : PACKAGESYMBOL ;
: : SN74LS08-DIP : AND2 : IC1 : 2 : : 1.cmp1 : 1B : PACKAGESYMBOL ;
: : SN74LS08-DIP : AND2 : IC1 : 3 : : 1.cmp1 : 1Y : PACKAGESYMBOL ;
```

### Reference

This Reference Manual on New Software Functions covers only optional parameters added to Rev. 6.0.

For details on **bdnetout**, see the User's Guide.

## ● Supporting cross-probing for multiple nets

### [Function]

With Rev. 5.0, you cannot select multiple nets on the PC board to send them to the schematic.

With Rev. 6.0, you can select multiple nets on the PC board and send selected net names to the SD.

### [Operation]

- (1) Select **Communicate** → **Layout Communication** from the SD menu bar.
- (2) Select **Communicate** → **Schematic Communication** → **On** from the BD menu bar.
- (3) Select **Attribute** → **Query Data** from the BD menu bar.
- (4) Set [Object Info] → [Net] in the panel menu.
- (5) Select multiple nets by specifying an area while touching the Shift key.
- (6) Select **Communicate** → **Transmit Selection Status** from the BD menu bar.

# 4-23 Test Point Function Expanded Added

The following functions are added or improved for the test point command.

- Function added to automatically extract test points
- Function to set and delete probe names
- Function to output a report
- Added sorting method for TP references
- Changed processing at test point occurrence

## ● Function added to automatically extract test points

### [Function]

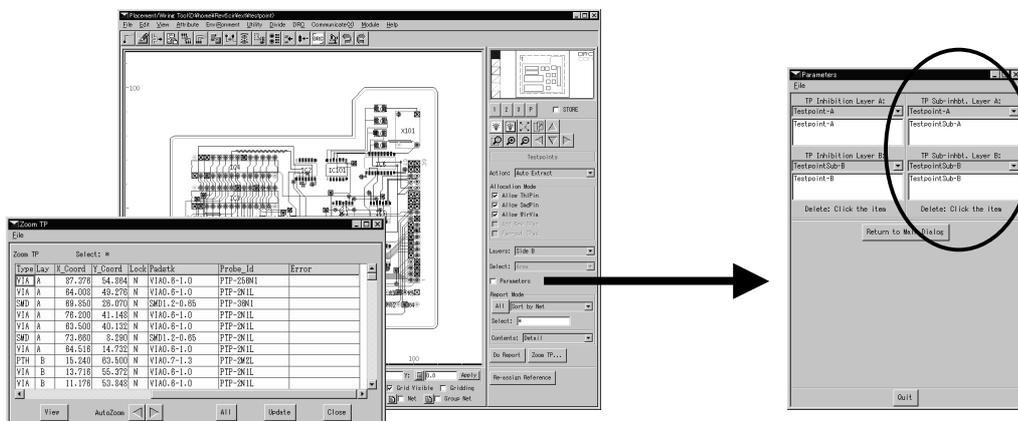
A function is added to set the test point attribute and probe names for padstacks by referring to the resource file for the TP probe containing probe names to generate and pitch between probes. The addition of this function enables the generation of a test point considering a probe.

In addition to the conventional test point inhibit layer in this function, a parameter is added to specify the test point sub-inhibit layer, an area where test point generation should be avoided as much as possible.

### <Resource file for TP probe>

- (1) \$HOME/cr5000/ue/tpprobe.rsc
- (2) \$SCR5\_PROJECT\_ROOT/ue/info/tpprobe.rsc
- (3) \$ZUEROOT/info/tpprobe.rsc

If multiple directories have this information, the system searches for the information in order from (1)→(2)→(3), referring to the file data first found.



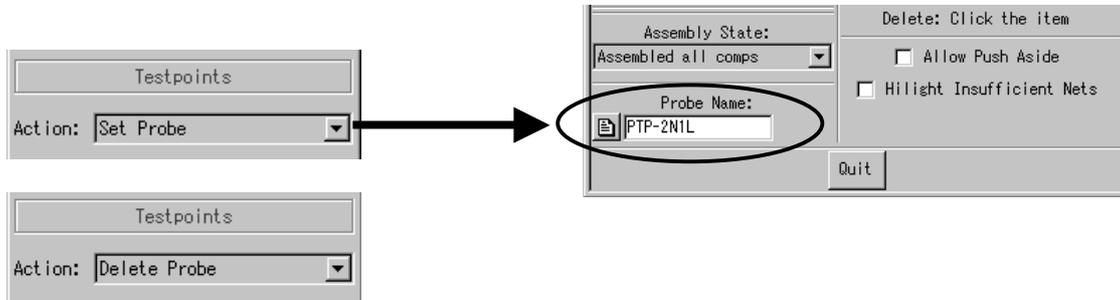
### [Notes and Restrictions]

- When you set a generation surface of “Both (A-side preference)” or “Both (B-side preference)” in the panel menu, automatic extraction cannot be executed.

## ● Function to set and delete probe names

### [Function]

The “automatic extraction” function enables the automatic setting of probe names as well as presetting of probe names to be set in the resource file for the TP probe so that you can manually set, change or delete probe names.



### [Notes and Restrictions]

- If a probe name is already set, the name is changed to the specified probe name.
- When you select a locked test point, an error occurs and setting and changing are not performed.
- You can only select “single.”

## ● Function to output a report

### [Function]

A function is added to output probe names set on “automatic extraction” and “probe setting” with the report output and TP zoom functions

Angle	Type	Layer	X_Coord	Y_Coord	Lock	Grid	Near_Pad	Probe_Id
0.0	VIA	A	87.378	54.884	N	Y	IC5(3)	PTP-258N1
0.0	VIA	A	84.888	49.278	N	Y	IC1(11)	PTP-2N1L
0.0	SMD	A	89.850	28.070	N	Y	IC8(3)	PTP-2N1L
0.0	VIA	A	76.200	41.148	N	Y	IC6(3)	PTP-2N1L
0.0	VIA	A	89.580	46.182	N	Y	IC7(5)	PTP-2N1L
0.0	SMD	A	79.880	9.290	N	Y	IC7(6)	PTP-2N1L
0.0	VIA	A	84.516	14.722	N	Y	IC7(11)	PTP-2N1L
0.0	PTH	B	15.240	63.500	N	Y	IC4(3)	PTP-2N1L
0.0	VIA	B	19.716	55.372	N	Y	IC3(25)	PTP-2N1L
0.0	VIA	B	23.940	58.420	N	Y	IC7(5)	PTP-2N1L
0.0	PTH	B	7.920	98.480	N	Y	UI(1)	PTP-2N1L
0.0	PTH	B	12.780	98.880	N	Y	IC5(2)	PTP-2N1L
0.0	PTH	B	15.240	98.480	N	Y	UI(4)	PTP-2N1L
0.0	PTH	B	38.400	71.720	N	Y	IC4(8)	PTP-2N1L
0.0	SMD	A	88.580	43.850	N	Y	IC1(2)	PTP-2N1L
0.0	VIA	A	40.752	46.200	N	Y	IC5(11)	PTP-258N1
0.0	VIA	A	49.278	49.278	N	Y	IC3(12)	PTP-2N1L
0.0	VIA	B	40.240	32.884	N	Y	UI(12)	PTP-2N1L
0.0	VIA	B	44.784	35.852	N	Y	UI(8)	PTP-2N1L

<Report output>

Near_Pad	Type	Layer	X_Coord	Y_Coord	Lock	Padatk	Probe_Id
IC5(3)	VIA	A	87.378	54.884	N	VIA0.6-1.0	PTP-258N1
IC1(11)	VIA	A	84.888	49.278	N	VIA0.6-1.0	PTP-2N1L
IC8(3)	SMD	A	89.850	28.070	N	SMD1.2-0.85	PTP-2N1L
IC6(3)	VIA	A	76.200	41.148	N	VIA0.6-1.0	PTP-2N1L
IC7(5)	VIA	A	89.580	46.182	N	VIA0.6-1.0	PTP-2N1L
IC7(6)	SMD	A	79.880	9.290	N	SMD1.2-0.85	PTP-2N1L
IC7(11)	VIA	A	84.516	14.722	N	VIA0.6-1.0	PTP-2N1L
IC4(3)	PTH	B	15.240	63.500	N	VIA0.7-1.3	PTP-2N1L
IC3(25)	VIA	B	19.716	55.372	N	VIA0.8-1.0	PTP-2N1L
UI(30)	VIA	B	11.178	53.848	N	VIA0.8-1.0	PTP-2N1L

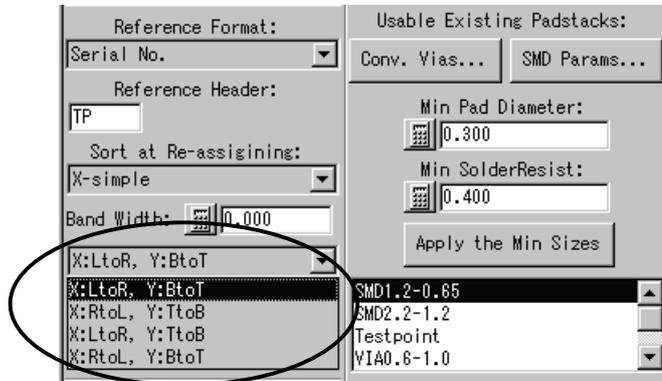
<TP zoom>

## ● Added sorting method for TP references

### [Function]

With Rev. 5.0, test point references are sorted from “From left/down” or “From right/up.”

With Rev. 6.0, “From left/up” and “From right/from down” are added to the conventional two.



### [Notes and Restrictions]

- When you have loaded data used with Rev. 5.0, the start point may be different from that selected before. Save data after selecting the start point.
- When you have loaded a parameter resource file used with Rev. 5.0, the start point may be different from that selected before. Output the parameter resource after selecting the start point.

## ● Changed processing at test point occurrence

### [Function]

Because Rev. 5.0 checks the placement keep-out area upon test point generation, you cannot set the test point attribute to a padstack in the placement keep-out area.

Because Rev. 6.0 differentiates the placement keep-out and test point keep-out, the placement keep-out area check is eliminated and the test point attribute becomes settable.

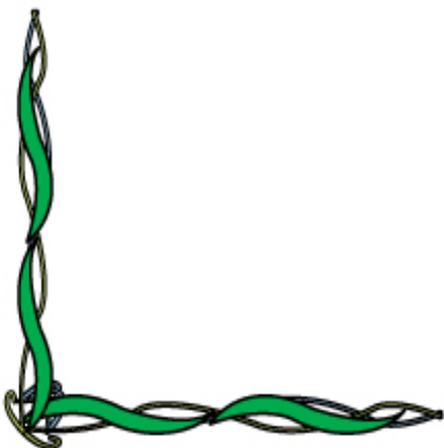
### [Notes and Restrictions]

- If you prohibited TPs in the placement keep-out area for Rev. 5.0 operation, input the same figure onto the test point keep-out layer for operation.



# Chapter 5

## Artwork Tool



# 5-1 Editing Conductive Layer



## [Function]

The Placement/Wiring Tool and Artwork Tool cover different ranges for design depending on layers in Rev. 5.0, and the Artwork Tool cannot input, edit or delete data for conductive layers (hereafter, conductive layer editing). As certain PC board types require general 2-D editing on conductive layers, the Rev. 6.0 Artwork Tool is improved to perform conductive layer editing.

### Supported commands

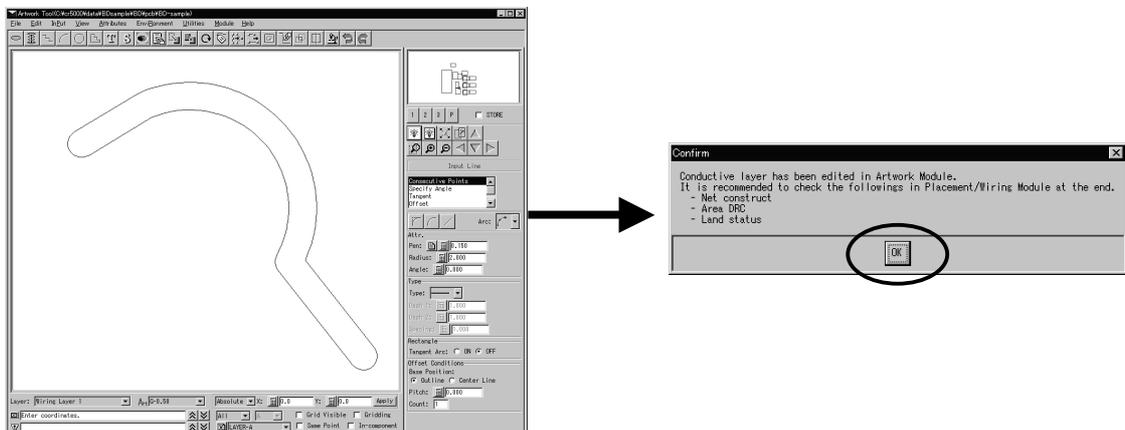
- |                   |                  |             |                      |
|-------------------|------------------|-------------|----------------------|
| •Input pad        | •Input line      | •Input arc  | •Input circle        |
| •Input surface    | •Input character | •Delete     | •Move                |
| •Copy             | •Rotate          | •Edit shape | •Extend/shorten line |
| •Add              | •Cut-out         | •Combine    | •Split               |
| •Change attribute |                  |             |                      |
- \*“Input padstack” and “Select” are available as before.

The Artwork Tool has some limits and points to be noted for conductive layer editing compared with the Placement/Wiring Tool due to its characteristics. So, when conductive layer editing is performed for the first time with the Artwork Tool, confirmation dialog boxes for “Build net,” “Area DRC” and “Land status” appear. These dialog boxes also appear at the following occasions.

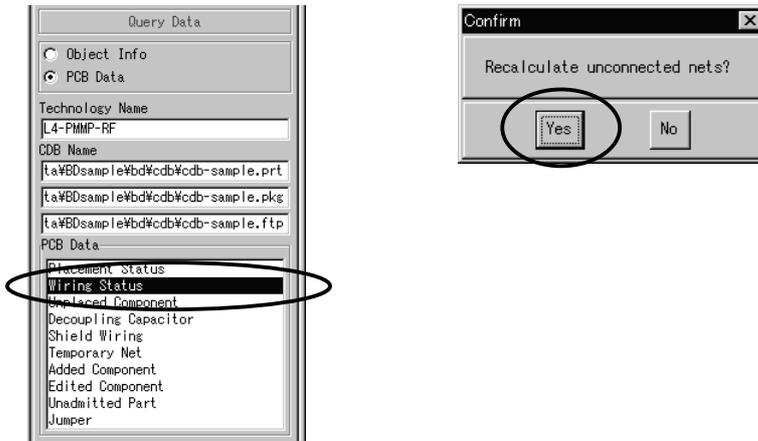
- |                         |                                              |                        |
|-------------------------|----------------------------------------------|------------------------|
| •When the tool is ended | •When modules are switched                   | •When a file is opened |
| •When a file is saved   | •When a file is saved under a different name |                        |

## [Operation]

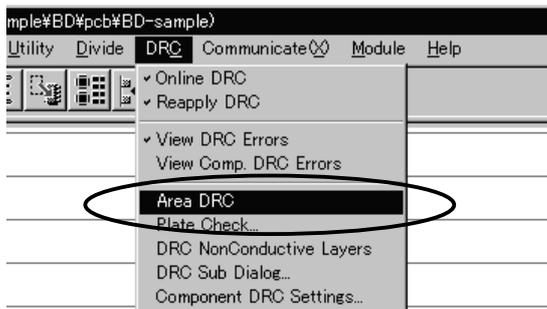
- (1) Select **Input** → **Line** from the menu bar.
- (2) Select a conductive layer to input from the active layer selector menu in the editing indicator at the bottom of the editor.
- (3) Input data and end the command.
- (4) After the confirmation dialog box appears, click **OK** to close the dialog box.



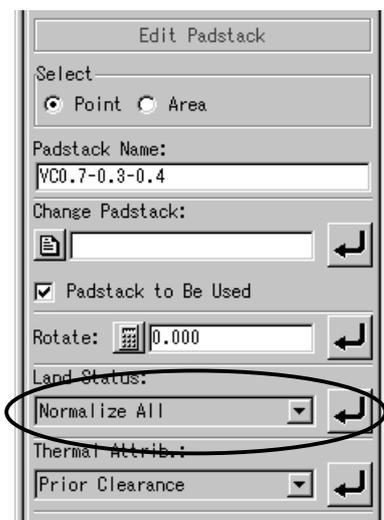
- To execute “Build net,” use the confirmation dialog box output when **Attribute** → **Query data** is selected from the Placement/Wiring Tool menu bar and then **Wiring Status** is selected in “PCB Data” in the panel menu.



- To execute “Area DRC,” select **DRC** → **Area DRC** from the Placement/Wiring Tool menu bar.



- To normalize “Land status,” select **Edit** → **Edit padstack** from the menu bar for the Placement/Wiring Tool, and then select **Normalize All** in “Land Status” in the panel.



## [Notes and Restrictions]

- The Artwork Tool does not normalize the land status for padstack. To normalize this, use the Placement/Wiring Tool.
- If you edit an object with net using the Artwork Tool, the net is maintained but not rebuilt.  
If edited or deleted objects had a net, the net is rebuilt when the module is switched to the Placement/Wiring or Floor Plan Tool.  
However, the net is not rebuilt at module switching after you input a new line to be retracted into a pin with net.
- Because the Artwork Tool does not support online DRC, the pen width may not satisfy the wiring width limit or the set maximum and minimum values. Therefore, execute Area DRC using the Placement/Wiring Tool.
- When a line is retracted into line segments, the Placement/Wiring Tool generates vertexes on the original line segments. If you deletes a line making up a T-junction, the remaining two lines are combined (the vertex disappears).  
The Artwork Tool does not carry out such maintenance for T-junctions.
- The net is not rebuilt unless the ends of lines overlap each other or a line-end overlaps a surface. Therefore, when a line is retracted into line segments or a line crosses over a surface, they are not regarded as a series of net even after net rebuilding. Note this point when editing with the Artwork Tool.
- The Artwork Tool does not support input, editing and deletion of mesh planes, hierarchy ports or divided areas.
- Although you can create a loop pattern with the Artwork Tool, note that the loop is deleted if you edit the data with the Placement/Wiring Tool in the loop disabled status.

---

## 5-2 Enhanced Check Function

---



The following functions are added or improved for the MRC command.

- Improved MRC command operability
- Improved Resist and metal mask missing checks
- Symbol mark attribute check
- MRC command supporting actual character shapes

### ● Improved MRC command operability

To improve MRC command operability, the following functions are added or improved.

- Deleting error marks at rechecking
- Selecting the rule pitch or local pitch
- File output function for the Error List dialog box

### Deleting error marks at rechecking

#### [Function]

If the MRC command is used for checking and error marks from a previous check remain in the area to check, Rev. 6.0 deletes these error marks before the check.

This prevents error marks from remaining at a correct point.

The following commands are supported.

- Resist design/resist missing check
- Resist design/multiple conductor enclosure check
- Resist design/resist adjacent check
- Resist design/PC board outline adjacent check
- Resist design/annular-ring check
- Symbol mark design/component symbol check
- Symbol mark design/resist overlap check
- Symbol mark design/metal mask overlap check
- Symbol mark design/hole overlap check
- Symbol mark design/component overlap check
- Symbol mark design/character overlap check
- Symbol mark design/conductor overlap check
- Metal mask design/metal mask missing check
- Metal mask design/metal mask adjacent check
- Metal mask design/annular-ring check
- Drill overlap check

#### [Notes and Restrictions]

- Symbol mark design/component symbol check deletes all error information regardless of whether the component is selected for check.

## Selecting the rule pitch or local pitch

### [Function]

You can select either the rule pitch or the local pitch to check the MRC command.

The following commands are supported.

- Resist design/multiple conductor enclosure check
- Resist design/resist adjacent check
- Symbol mark design/resist overlap check
- Symbol mark design/hole overlap check



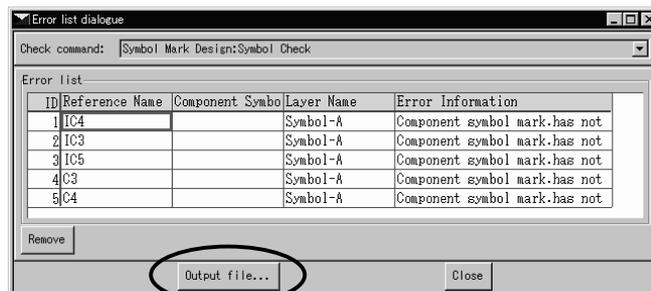
### [Notes and Restrictions]

- Even if you select the rule pitch, you cannot edit the design rule.

## File output function for the Error List dialog box

### [Function]

You can output data displayed in the Error List dialog box to a text file.

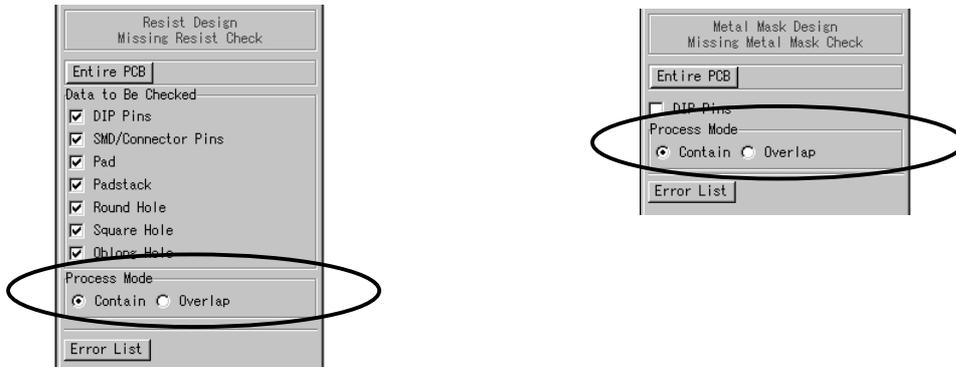


```
### Symbol Mark Design/Symbol Check ###
+---+-----+-----+-----+-----+
|ID|Reference Name|Component Symbo|Layer Name|Error Information|
+---+-----+-----+-----+-----+
|1|IC4| |Symbol-A|Component symbol mark.has not|
+---+-----+-----+-----+-----+
|2|IC3| |Symbol-A|Component symbol mark.has not|
+---+-----+-----+-----+-----+
|3|IC5| |Symbol-A|Component symbol mark.has not|
+---+-----+-----+-----+-----+
|4|IC3| |Symbol-A|Component symbol mark.has not|
+---+-----+-----+-----+-----+
|5|IC4| |Symbol-A|Component symbol mark.has not|
+---+-----+-----+-----+-----+
```

## ● Improved Resist and metal mask missing checks

### [Function]

The enclosure and overlap check modes are added to the resist and metal mask missing check commands to check for resists and metal masks overlapping of the target data. The enclosure check checks if the target data is completely within a resist or metal mask. The overlap check checks if the target data overlaps a resist or metal mask.



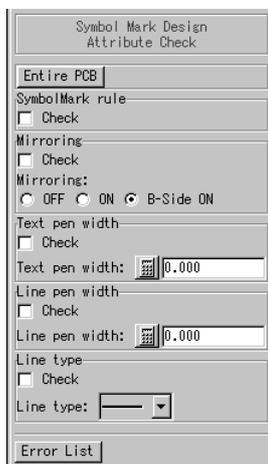
## ● Symbol mark attribute check

### [Function]

To enhance the MRC command function, Rev. 6.0 enables checking of the following items for symbol marks.

- Minimum character width set by a design rule, symbol mark rule
- Minimum character height
- Minimum character interval
- Existence of a symbol mark character not conforming to the character angle limit
- Mirroring attribute check for symbol mark character data
- Character minimum pen width check for symbol mark character data
- Minimum pen width check for symbol mark line data
- Line type check for symbol mark line data

Click Utility → Symbol Mark Design → Symbol mark attribute check from the menu bar.



## ● MRC command supporting actual character shapes

### [Function]

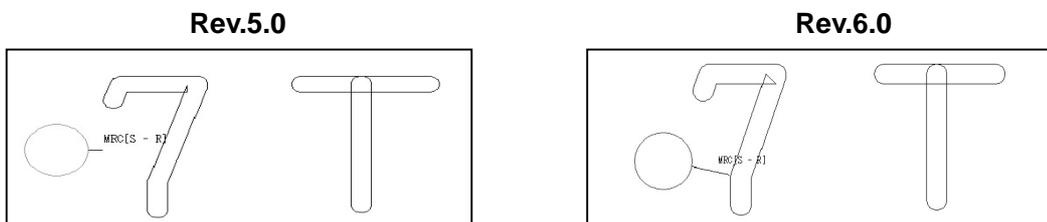
Rev. 5.0 uses the character bounding box to check character data.

With Rev. 6.0 enables direct checking with the actual character shape, realizing checking with accurate clearance.

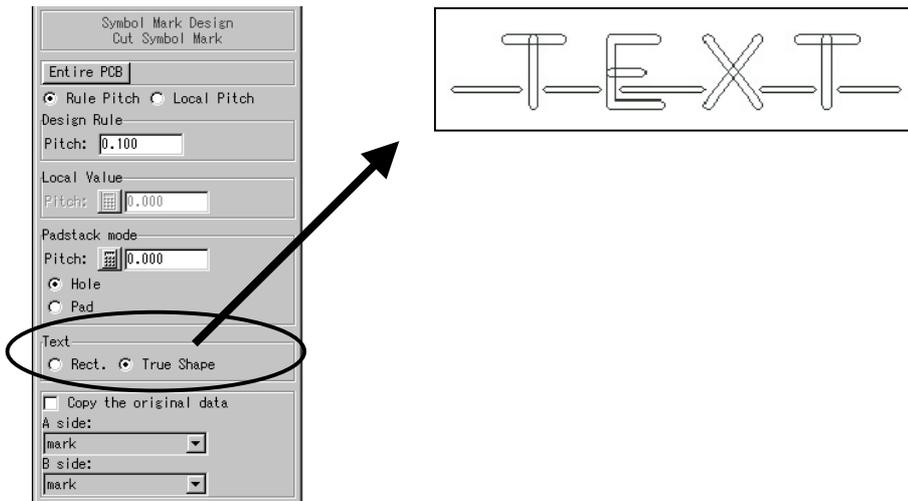
The following commands are supported.

- MRC command
- Symbol mark cut command
- Ruler function for the Query command

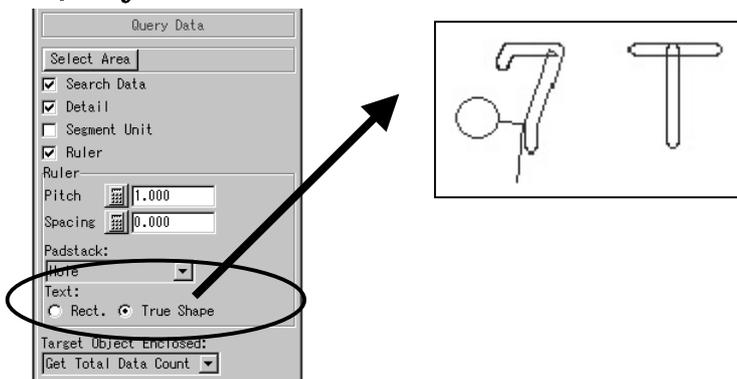
### <Symbol mark design resist overlap check>



### <Symbol mark cut command>



### <Query command>



---

## 5-3 Enhanced Input and Edit Function

---



The following functions are added or improved for the input and edit functions.

- General 2-D commands
- Commands supporting expanded hole-type numbers
- Function to add a thermal attribute upon padstack input
- Function added to specify a base position upon line offset input
- Function added to select an arc input mode
- Added automatic tangent arc generation mode upon rectangle input
- Simplifying offset specification
- Added successive drag copy mode
- Function added to convert a tangent arc to an arc upon attribute changing
- Specifying the character font table number upon attribute changing
- Added function for the cutout figure command
- Improved functions for the Query command
- Improved functions for the Object Import command

### ● General 2-D commands

#### [Function]

General 2-D commands representing functions useful in inputting and editing complicated figures are added.



From the left on the upper row

- Input line with specified angle
- Input tangent
- Input common tangent
- Input rectangle
- Input temporary bundle

From the left on the lower row

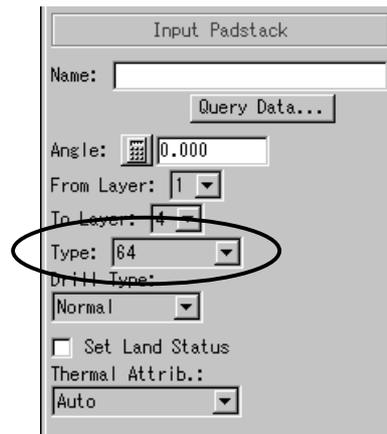
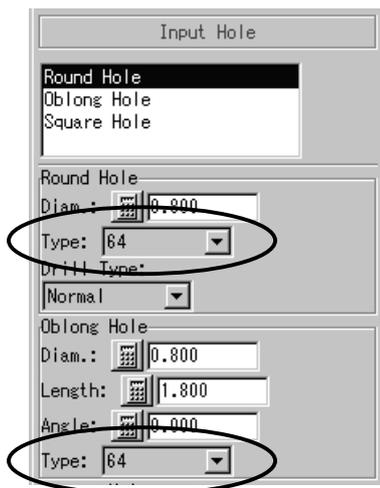
- Input parallel or horizontal line
- Trim line
- Convert surface line
- Convert line surface
- Combine line

## ● Commands supporting expanded hole-type numbers

### [Function]

The following Artwork Tool commands support the new upper limit on the hole-type numbers, which is raised from 15 to 64.

- Input padstack
- Input hole (round hole, oblong hole)
- Change padstack attribute
- Change round hole attribute
- Change oblong hole attribute
- Change attribute by specifying an area
- Hole diagram
- Query data
- Padstack area search rule
- Round hole area search rule
- Oblong hole area search rule

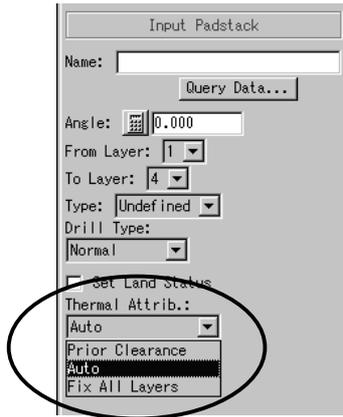


## ● Function to add a thermal attribute upon padstack input

### [Function]

You can input data with a “thermal attribute” upon padstack input.

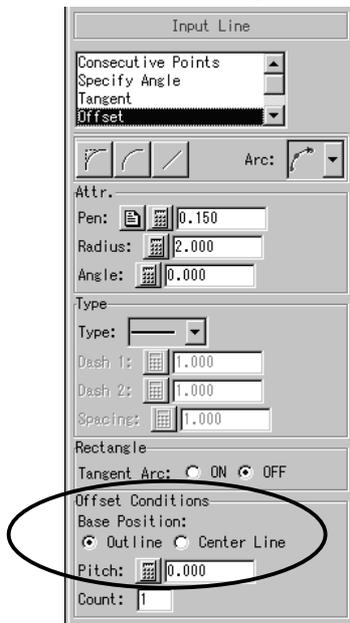
When an installation hole registered in the padstack is moved to the Placement/Wiring Tool in Rev. 5.0 or older, it is thermally connected to the Full Surface layer automatically. As a result, a net can be unintentionally set or other problems can occur. If you have fixed the thermal attribute at input, you can prevent automatic connection.



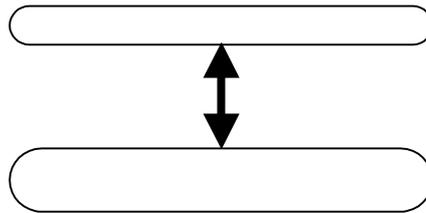
## ● Function added to specify a base position upon line offset input

### [Function]

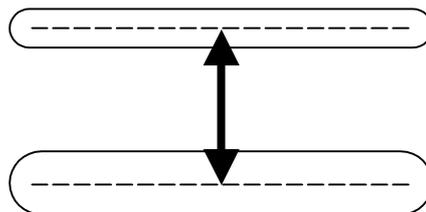
With Rev. 6.0, you can specify “Base Position” in the [Offset] mode at line input.



#### Line base position: outline



#### Line base position: centroid



### [Notes and Restrictions]

- The “Base Position” setting is only valid when the reference object is a line.  
The base position for surface is always its outline.

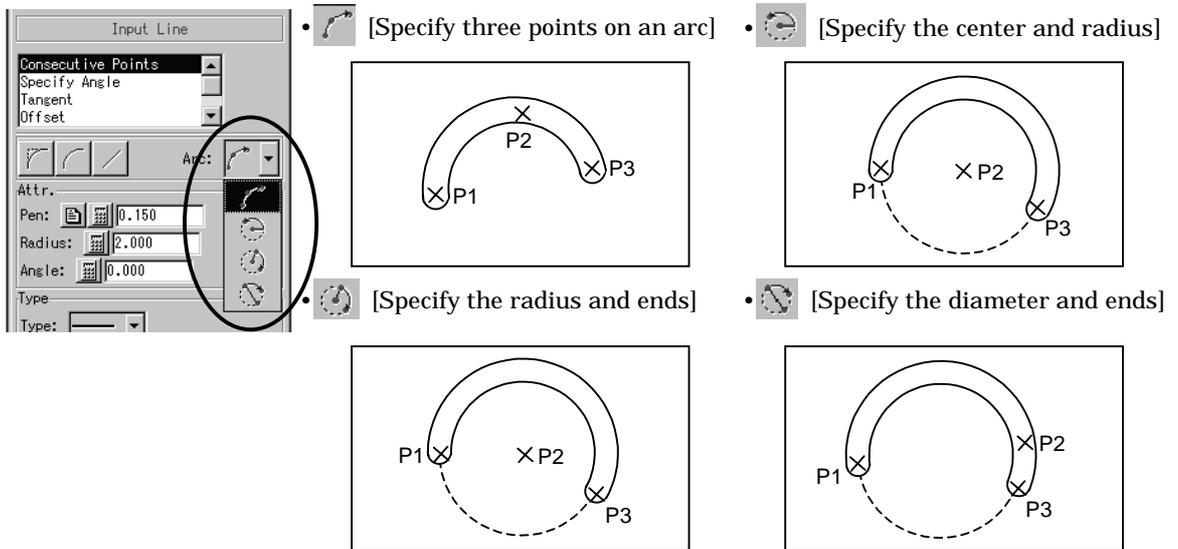
## ● Function added to select an arc input mode

### [Function]

With Rev. 6.0, you can select an “arc input mode” when inputting an arc with specified “Consecutive Points.” The supporting command are as follows.

- Consecutive Points for line input
- Consecutive Points for surface input
- Edit mode for shape editing
- Add command

The arc input mode is referred to when  [arc] is selected from the panel menu.



### [Notes and Restrictions]

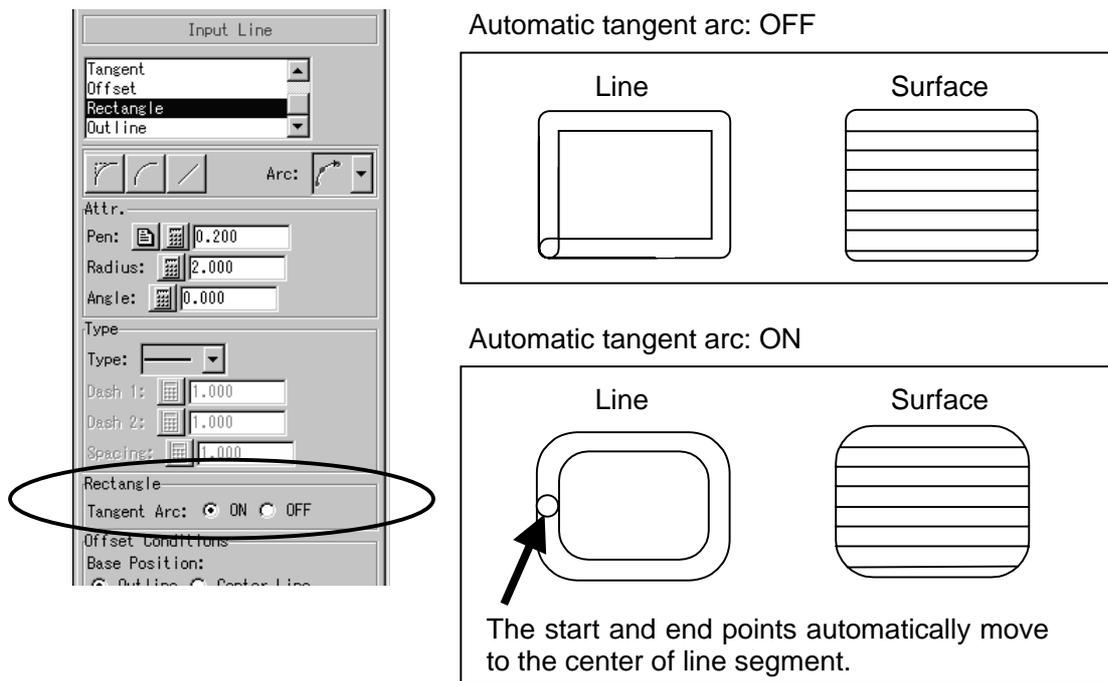
- You cannot change the arc input method in the waiting status for arc end point input (after you specify P2). In this case, the error message “Cannot change Arc Type during arc input.” appears.

## ● Added automatic tangent arc generation mode upon rectangle input

### [Function]

A function is added to generate an automatic tangent arc at the corner of a rectangle when a line or surface is input in the [Rectangle] mode.

When you input a rectangle line on a previous version, the start and end points for a line were generated at the corner. Therefore, it was impossible to generate an arc after input. This function reduces operation.



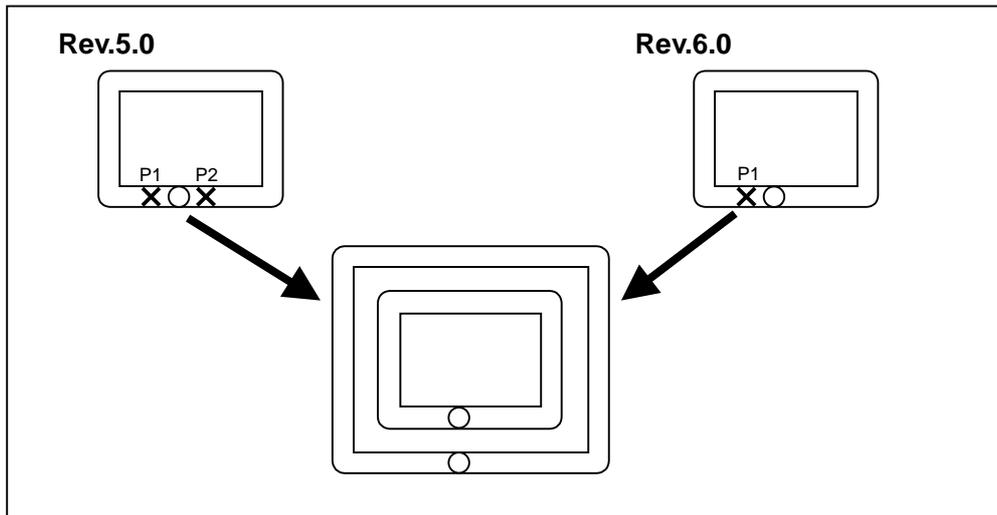
### [Notes and Restrictions]

- You can switch by selecting  [automatic tangent arc] or  [straight line] from the panel menu only when the command mode is Rectangle.
- If you input a line or surface when ON is set to Automatic Tangent Arc, the radius should be larger than half of pen width. The corresponding error message is "The automatic tangent arc radius is smaller than half of pen width."

## ● Simplifying offset specification

### [Function]

Operation to specify the entire line in the [Offset] mode for line input or surface input is simplified. With previous versions, you had to specify the start and end points of a line for offset input. In contrast, offset input for the entire line is possible with Rev. 6.0 if you specify a point and select [Data End].



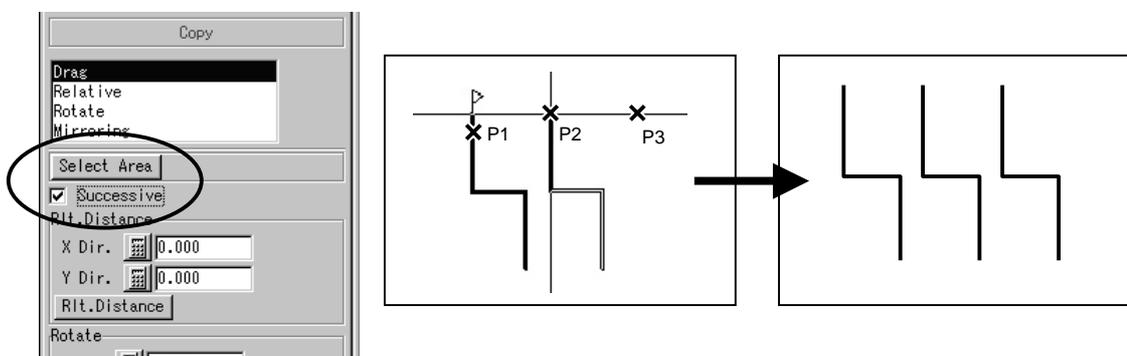
### [Notes and Restrictions]

- If you want to set offset to a line and then select other lines, specify two points (the start point and end point) for the first line. Selecting one point for the second or following lines does not set offset to them.

## ● Added successive drag copy mode

### [Function]

The successive copy function is added as the drag copy mode for the copy command. If the [Successive] check box in the panel menu is selected, you can repeat copying until [Data End] is selected.



### [Notes and Restrictions]

- Undo and Redo processing is performed in successive copy units.

● **Function added to convert a tangent arc to an arc upon attribute changing**

**[Function]**

While changing an attribute for a single line, surface, area or rule area, you can convert the vertexes for the tangent arc attribute to an arc with the same radius.

Change Line Attribute

Show Info  
Layer Name: mark  
Object Type: On Board

Change as a Whole  
Attr.: Middle Point->Tangent Arc  
Tangent Arc Radius: [input field]  
F. Wide Wid.: [input field]  
Fillet Len.: [input field]  
F. Narrow Wid.: [input field]  
Set to Table

No.	Coordinates	Line Width	Attribute	Radius	F.
1	(5.000, 8.000)	0.200	Start Point		
2*	(5.000, 11.000)	0.200	Tangent Arc	2.000	
3	(13.000, 11.000)	0.200	Tangent Arc	2.000	
4	(13.000, 5.000)	0.200	Tangent Arc	2.000	
5	(5.000, 5.000)	0.200	Tangent Arc	2.000	
6	(5.000, 8.000)	0.200	End Point		

Attribute List

- Tangent Arc
- Middle-Fillet to Arc
- to Arc

Cancel

Selecting **Apply** converts to arc.

No.	Coordinates	Line Width	Attribute	Radius	F. Wid
1	(5.000, 8.000)	0.200	Start Point		
2*	(5.000, 9.000)	0.200	Arc Start	2.000	
3	(7.000, 9.000)	0.200	Arc Center		
4	(7.000, 11.000)	0.200	Arc End		
5	(13.000, 11.000)	0.200	Tangent Arc	2.000	
6	(13.000, 5.000)	0.200	Tangent Arc	2.000	
7	(5.000, 5.000)	0.200	Tangent Arc	2.000	
8	(5.000, 8.000)	0.200	End Point		

**[Notes and Restrictions]**

- You cannot convert an arc into an automatic tangent arc.
- The Attribute List dialog box lists attribute names corresponding to the current attribute.

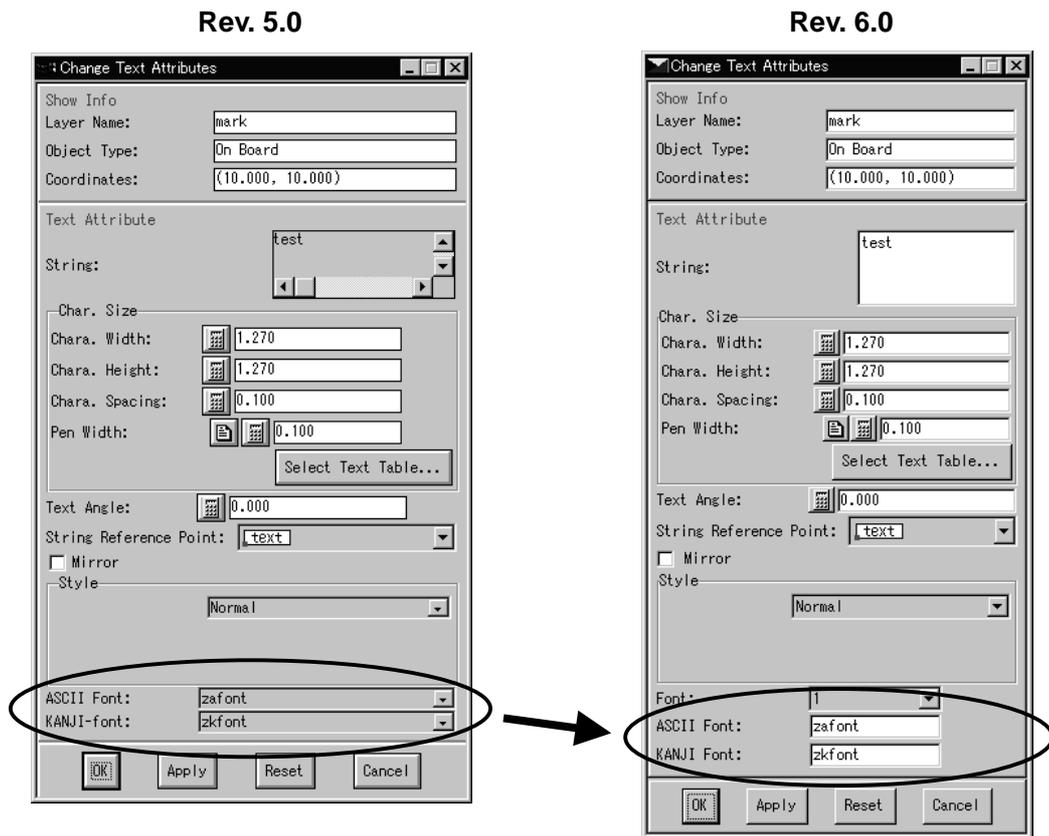
Example: For “Automatic tangent arc,” “→arc”

For “Start point of window or automatic tangent arc,” “→window start point arc”

## ● Specifying the character font table number upon attribute changing

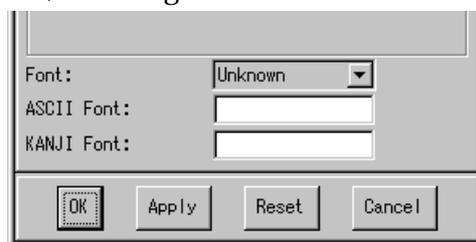
### [Function]

With Rev. 5.0, you can select ASCII font or Kanji font for each character to change the font. With Rev. 6.0, you can specify a font table number the same as with the input command for the CDB and Artwork Tool.



### [Notes and Restrictions]

- If a font not corresponding to a table number has been used, "Unknown" is displayed in the Font: field. If you change another attribute while leaving "Unknown" as-is, no change is reflected.



## ● Added function for the cutout figure command

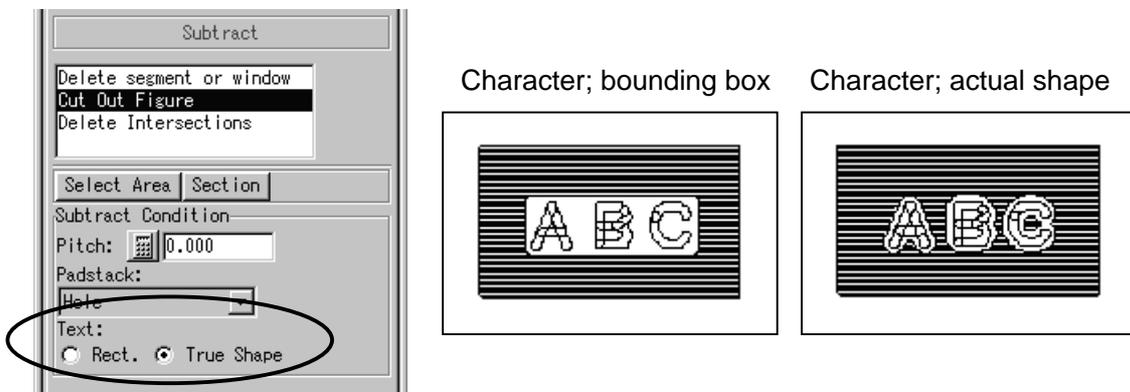
The following functions are added for the Cutout Figure command.

- Function to cut out an actual character shape
- Function to cut out a padstack

### Function to cut out an actual character shape

#### [Function]

When you try to cut out a character with Rev. 5.0, the rectangle enclosing the character is cut out. In contrast, a mode to cut out the actual character shape is added in Rev. 6.0.



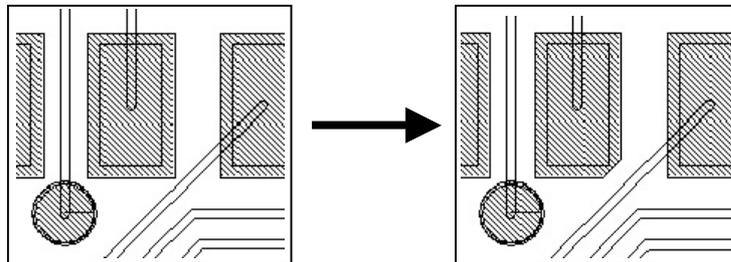
#### [Notes and Restrictions]

- The dimension character cannot be cut out.

### Function to cut out a padstack

#### [Function]

With Rev. 5.0, you can cut out only lines, surfaces and areas. With Rev. 6.0, you can cut out a figure in the pad and padstack, as well. This facilitates pad and padstack editing.



#### [Notes and Restrictions]

- You cannot cut out the whole pad shape in the conductive layer padstack.

## ● Improved functions for the Query command

The following points are improved for the Query command.

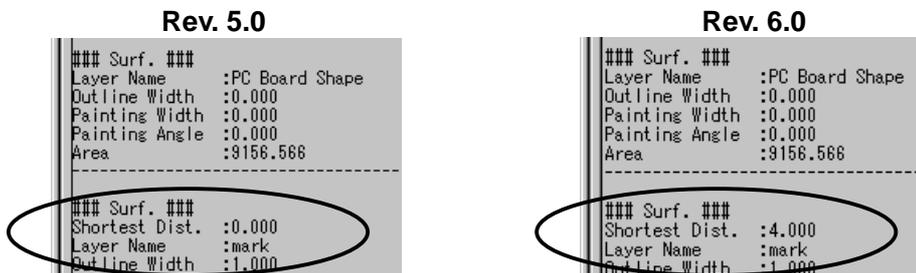
- Improved ruler function
- Added query information

### Improved ruler function

#### [Function]

With Rev. 5.0, you cannot measure the distance between PC board outline or layout area and an object within it by using the ruler function.

With Rev. 6.0, you can measure such a distance (for PC board outline and layout area only).

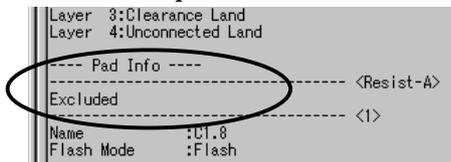


### Added query information

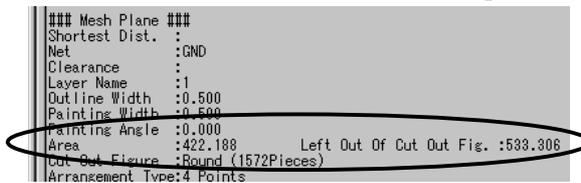
#### [Function]

The following new information is output upon data query.

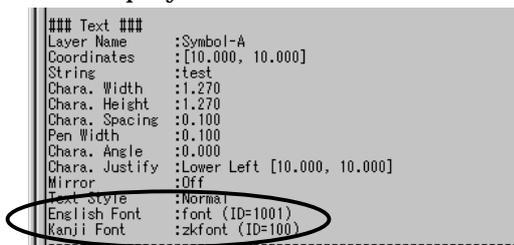
- Excluded pad information in the padstack



- Accurate area calculation of mesh plane and display of the number of cutout figures



- ID display when a font does not have any font name.



### [Notes and Restrictions]

- Excluded pad information does not cover information on layers without technology mapping.

## ● Improved functions for the Object Import command

The following functions are improved for the object import command.

- Function added to input by specifying coordinates
- Function added to specify a scale value
- Supporting input with photo equipment name undefined
- Clearing the limit on same layer-type filter at layer import

### Function added to input by specifying coordinates

#### [Function]

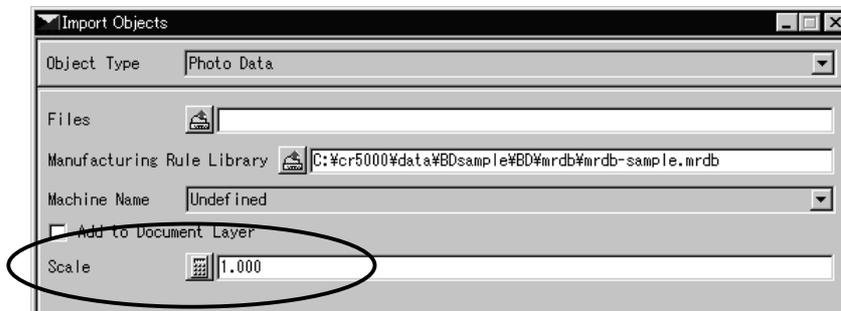
When you import an object in [Photo data] and [HP- GL, HP- GL/2] formats on Rev. 5.0, data is automatically imported into the origin position when [Execute] is clicked. Therefore, it is impossible to input data to a position other than the origin.

When [Execute] is clicked on Rev. 6.0, the maximum rectangle enclosing data follows the cursor enabling you to specify an arbitrary point and import it.

### Function added to specify a scale value

#### [Function]

With Rev. 6.0, you can specify a scale value when importing an object in [Photo data] and [HP- GL, HP- GL/2] formats.



#### [Notes and Restrictions]

- Scale value should be from 0.00001 to 19900.0.

### Supporting input with photo equipment name undefined

#### [Function]

With Rev. 6.0, you can import a [Photo data] object even if the photo equipment name is undefined.

The system analyzes the format of target photo data for import.

#### [Notes and Restrictions]

- The system cannot analyze some photo data formats. In this case, specify photo equipment name before importing.

## Clearing the limit on same layer-type filter at layer import

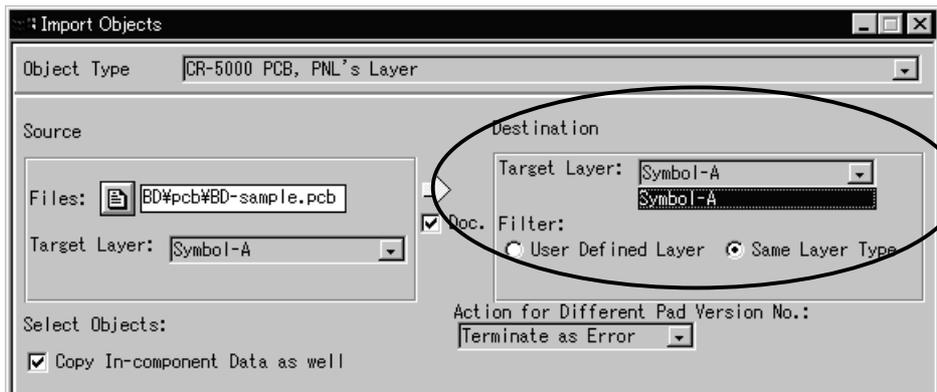
### [Function]

The Target Layer filter specifications used by the import command when [CR-5000 PCB, PNL's Layer] is selected as Object Type and [Same Layer-Type] is selected as target filter are changed.

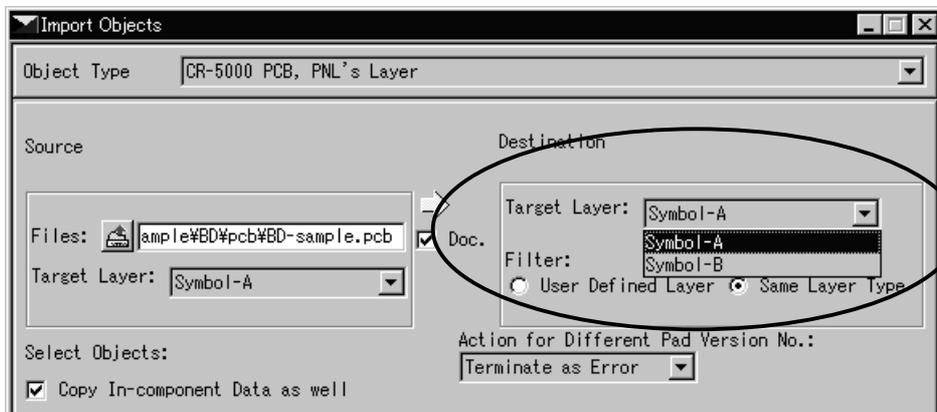
When you select [Same Layer-Type] in Rev. 5.0, the filter lists the layer with the same type and the same placement side as the original layer and, therefore, a layer is not displayed just because it is of the same type.

With Rev. 6.0, all same type layers are listed.

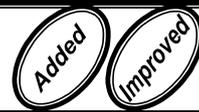
### Rev. 5.0



### Rev. 6.0



## 5-4 Hole Drawing Command



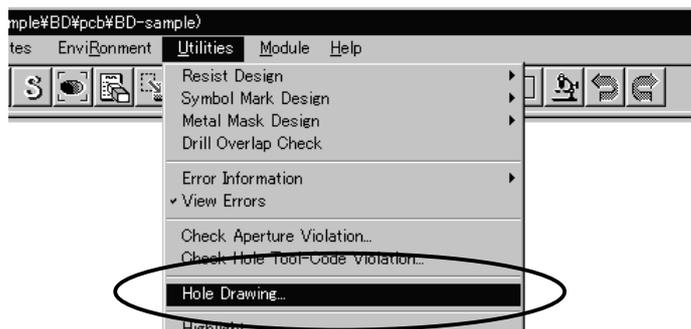
The following functions are added or improved for the Hole Drawing command.

- Built into the Artwork Tool
- Layer to input changed
- Added generation character parameter
- Printing non-generated data list
- Output list
- Restoring parameters upon [Load All Hole Rules] execution
- Panel operation supporting from\_to in the sub-PC board

### ● Built into the Artwork Tool

#### [Function]

Although the hole drawing command can be executed with the Manufacturing Panel Design Tool on previous versions, you can execute it with the Rev. 6.0 Artwork Tool.



#### [Notes and Restrictions]

- A hole that is not developed on the sub-PC board is not covered by hole-drawing.

### ● Layer to input changed

#### [Function]

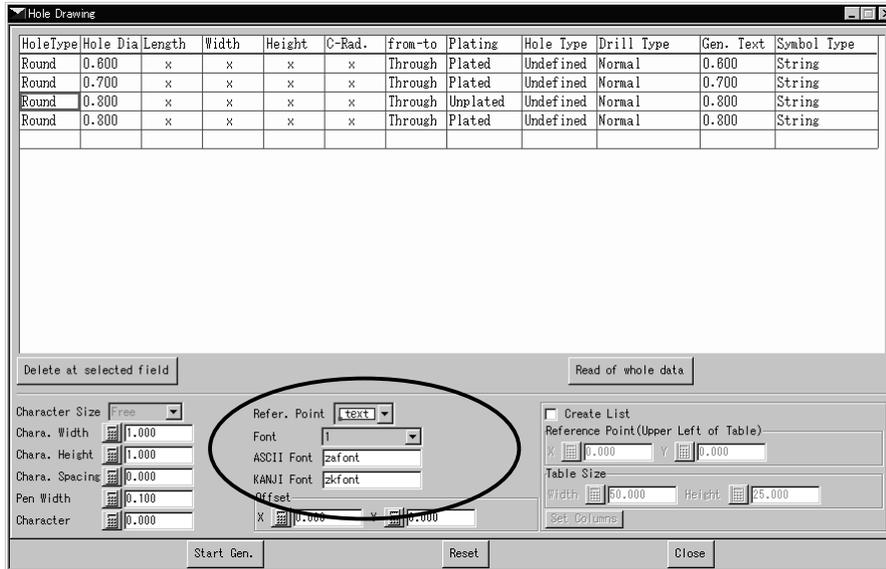
Specifications are changed to prohibit inputting a hole onto a conductive layer.

## ● Added generation character parameter

### [Function]

With Rev. 6.0, you can specify the following items.

- Character reference point
- Character font



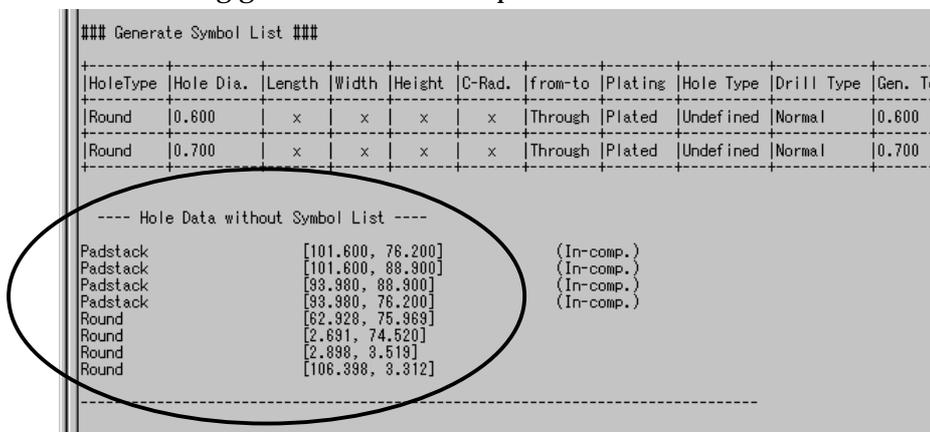
### [Notes and Restrictions]

- Specified “reference point” and “font” are applied to all generated character strings.

## ● Printing non-generated data list

### [Function]

The list of non-generated data is displayed so that you can see for which hole data hole-drawing generation was not processed.



### [Notes and Restrictions]

- This lists holes for which processing was not performed on the last execution and includes holes that have been already generated.

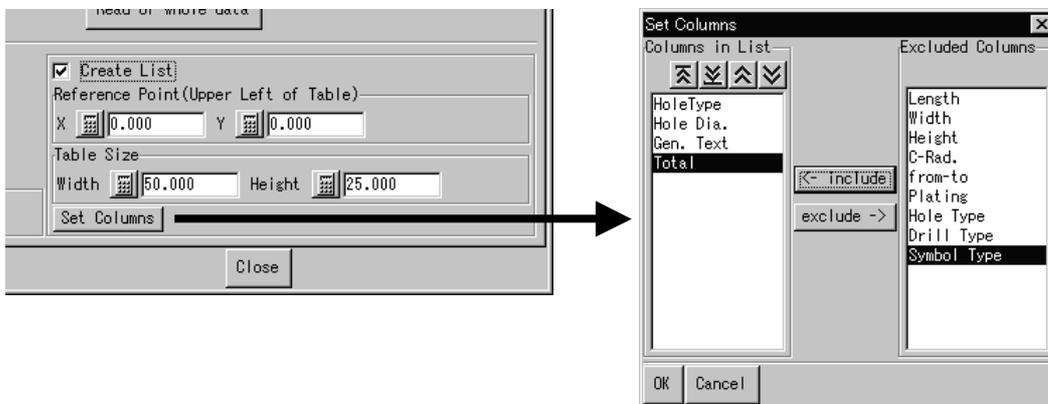
## ● Output list

### [Function]

You can output the list on the PC board when hole-drawing is generated. The list is output to the same active layer containing the hole drawing.

HoleType	Hole Dia.	Gen. Text	Total
Round	0.600	0.600	50
Round	0.700	0.700	186
Round	0.800	0.800	4
Round	2.000	2.000	5

You can specify the position, size and output items for the list.



### [Notes and Restrictions]

- The sizes of characters and pads change as the size of the specified table changes.  
If a pad is scaled, the pad becomes “edited.”
- If a pad without shape (pad not copied from CDB) is specified, the pad name is output as a character.
- The character font for list is “\_zafont0” for 1-byte characters and “zkfont” for 2-byte characters and they cannot be changed. (In the Korean environment, the 2-byte character font is “zhangul.”)

## ● Restoring parameters upon [Load All Hole Rules] execution

### [Function]

If hole-drawing parameters are defined in the parameter resource file on Rev. 5.0, [Load All Hole Rules] clears the entire parameter resource file and then loads the hole diameter on the PC board. Therefore, you cannot make use of the rules set in the resource file.

Rev. 6.0 has improved function to load non-existent hole rules, maintaining definition in the parameter resource. This enables defining of general hole diameters in the resource file and makes efficient use of them.

Execute [Load All Hole Rules]

HoleType	Hole Dia	Length	Width	Height	C-Rad.	from-to	Plating	Hole Type	Drill Type	Gen. Text	Symbol Type
Round	0.400	x	x	x	x	Through	Unplated	Undefined	Normal	0.4	String
Round	0.600	x	x	x	x	Through	Plated	Undefined	Normal	0.6	String
Round	0.700	x	x	x	x	Through	Plated	Undefined	Normal	0.7	String

HoleType	Hole Dia	Length	Width	Height	C-Rad.	from-to	Plating	Hole Type	Drill Type	Gen. Text	Symbol Type
Round	0.400	x	x	x	x	Through	Unplated	Undefined	Normal	0.4	String
Round	0.500	x	x	x	x	Through	Unplated	Undefined	Normal	0.500	String
Round	0.600	x	x	x	x	Through	Plated	Undefined	Normal	0.6	String
Round	0.700	x	x	x	x	Through	Plated	Undefined	Normal	0.7	String
Round	2.000	x	x	x	x	Through	Unplated	Undefined	Normal	2.000	String

While the existing rules are maintained, non-existent ones are added.

### [Notes and Restrictions]

- To delete unnecessary rows, click the hole-type cell and select [Delete the Specified Field Item]. You can select multiple rows with [Ctrl] + double-click or [Shift] + double-click.

## ● Panel operation supporting from\_to in the sub-PC board

### [Function]

If you change a sub-PC board from\_to layers loaded on the panel, Rev. 5.0 refers to the original sub-PC board from\_to layers, making it impossible to generate a correct hole drawing on the sub-PC board.

Rev. 6.0 loads and generates a hole by referring to that loaded on the panel.

### [Notes and Restrictions]

- If the FROM layer or TO layer of a sub-PC board is not connected to a panel, a hole drawing is not generated. In this case, the following dialog box appears to notify the user.



# 5-5 Component Operations



The following functions are added for component operation.

- Function added to specify component input reference
- Component input scaling permission

## ● Function added to specify component input reference

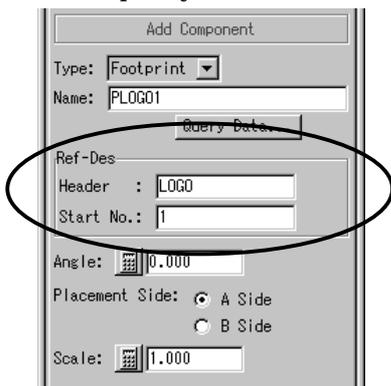
### [Function]

When you generate a component using the Artwork Tool or Manufacturing Panel Design Tool in Rev. 5.0, the system automatically allocates references, for example, cam1, cam2, cam3... These are difficult to understand.

With Rev. 6.0, you can specify the header and the first number for references.

### [Operation]

- (1) Click **Edit** → **Component Operation** → **Input** from the menu bar.
- (2) Specify values for [Header:] and [Start No.:] under Ref-Des in the panel menu.



- (3) Input a component.



### [Notes and Restrictions]

- You do not have to specify a header. Although you can specify numbers as the header, note that they cannot be differentiated as header once a component is input.
- You can specify for example, 01 or 001 as the first reference number. When you specify 01, 09 is followed by 10, 11, 12...
- The following items are added in the parameter resource (parameter.rsc).

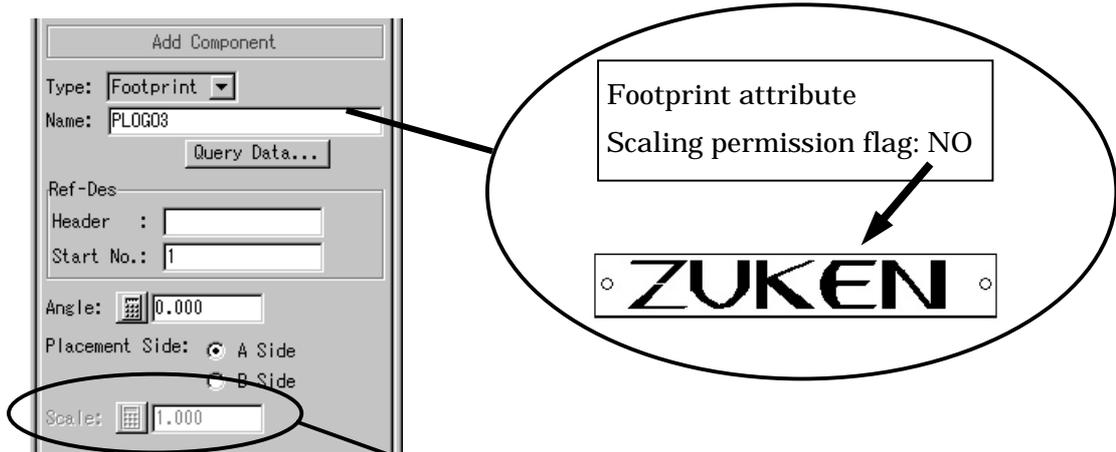
Parameter	Explanation
Artwork.Component.refdes.header	Reference header
Artwork.Component.refdes.startno	First reference number

## ● Component input scaling permission

### [Function]

Rev. 5.0 enables scaling of non-schematic components for input. However, because you were allowed to scale all components, such as component containing a hole, you could scale such a component by mistake causing failure upon drill output.

To prevent this inconvenience, Rev. 6.0 has the new scaling permission flag (Attribute name: Scaling, attribute value: YES or NO) in footprint attribute at footprint registration, so that you can decide whether to permit scaling upon component input.

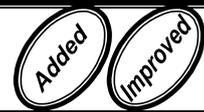


Scaling Permission Flag: If a footprint with NO is selected, the scaling icon is shaded and unavailable.

### [Notes and Restrictions]

- The footprint attribute is referred to when a component is input with [Type : part] specification.
- You can input a schematic component using the Manufacturing Panel Design Tool. However, you cannot scale a schematic component even if the scaling permission flag is set to YES.
- When the scaling permission flag is undefined for a component, the default is YES and scaling is possible.

# 5-6 Other Improvements



The following functions are added or improved for the Artwork command.

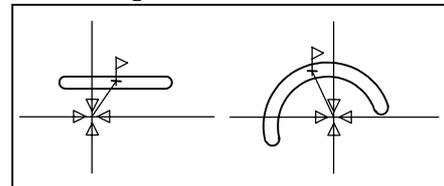
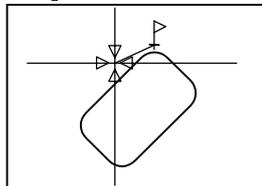
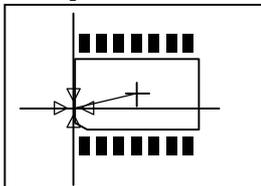
- Added same point candidate
- Keep-out and height limit area layers added to the active layer
- Object search mode reference
- Improved visibility at area selection

## ● Added same point candidate

### [Function]

The following data are used as the same point candidate on Rev. 6.0.

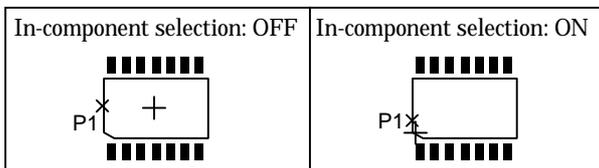
- Component reference point
- Square hole corner
- Line segment center



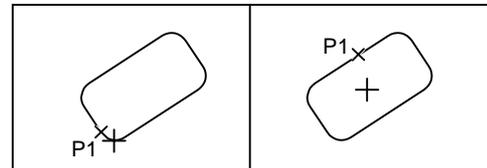
With previous versions, you have to specify the start and end points of an arc to select the arc center as the same point function. With Rev. 6.0, you just have to select an arbitrary point on an arc line segment to select the center.

The searched point differs depending on the specified point.

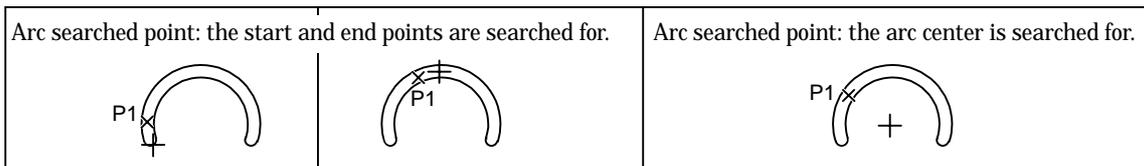
#### <Component>



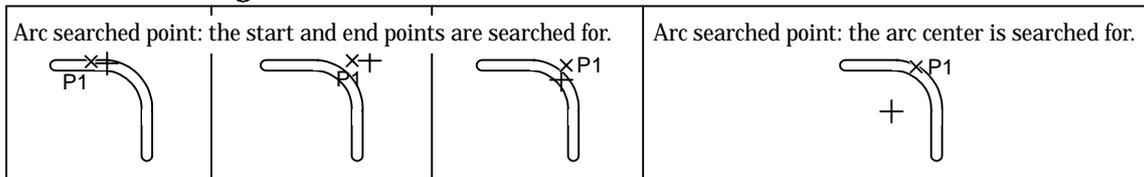
#### <Square hole>



#### <Arc>

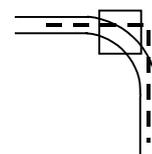


#### <Automatic tangent arc>



### [Notes and Restrictions]

- To search for the top, middle point or the center of an automatic tangent arc, the line segments between the tangent arc top and the end vertexes of the tangent arc should be contained in trap.



## ● Keep-out and height limit area layers added to the active layer

### [Function]

The following layers are added and can be edited as the active layer for the Artwork Tool.

- Wiring keep-out layer
- Placement keep-out layer
- Via keep-out layer
- Wiring and Via keep-out layer
- Height limit area layer

Although these layers cannot be edited with tools other than the PC Board Outline Edit Tool, the Rev. 6.0 Artwork Tool supports them and edit figures input onto these layers in the component.

### [Notes and Restrictions]

- You can input only lines and surfaces into the keep-out layer and you cannot input dashed-lines, chained-lines, or line with fillet with 0 pen width or length.
- You can input only area (surface input) onto the height limit area layer.

## ● Object search mode reference

### [Function]

With Rev. 5.0, the single object search mode is referred to by only some commands (copy, move, rotate, delete, change attribute and request), making operation complicated.

With Rev. 6.0, all commands refer to the object search mode. In other word, you can select this for any command.

### [Notes and Restrictions]

- Each check command for the Artwork Tool does not refer to the object search mode.

## ● Improved visibility at area selection

### [Function]

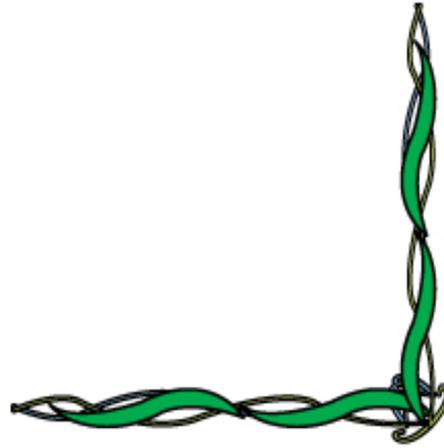
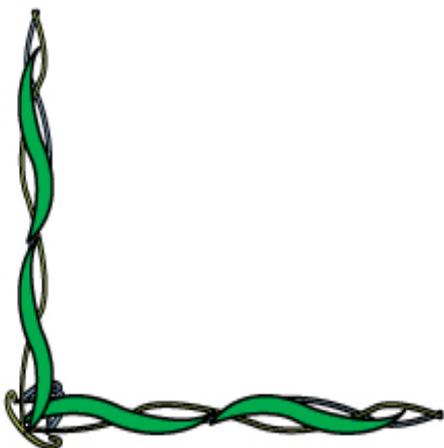
Visibility is improved when you select the second point after the first point at area selection.





# **Chapter 6**

## **Manufacturing Panel Design Tool**



# 6-1 Enhanced Manufacturing Panel Design Tool Function



The following functions are added or improved for the Manufacturing Panel Design Tool.

- Changed sub-PC board path
- Reference display
- Reference overlap check
- PC board input reversion function made an option

## Reference

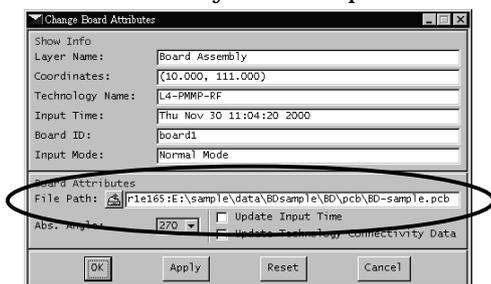
This chapter explains only functions specific to the Manufacturing Panel Design Tool. See “Chapter 5 Artwork Tool” as well.

### ● Changed sub-PC board path

#### [Function]

To replace a sub-PC board input onto the panel on Rev. 5.0, you have to delete the sub-PC board and input a new one.

With Rev. 6.0, you can replace sub-PC boards by changing their file path.



#### [Notes and Restrictions]

- You cannot replace using a sub-PC board with different technology.
- You cannot change the settings for “File Path” and “Update Technology Connectivity Data” at the same time.

### ● Reference display

#### [Function]

You can display references for panel components and components on the placement PC board by placement side.

#### [Operation]

- (1) Select **View** → **Reference** → **On** from the menu bar to display references.
- (2) Select **View** → **Reference** → **Display surface** → **Both/A-side/B-side** to specify a component placement side to display.

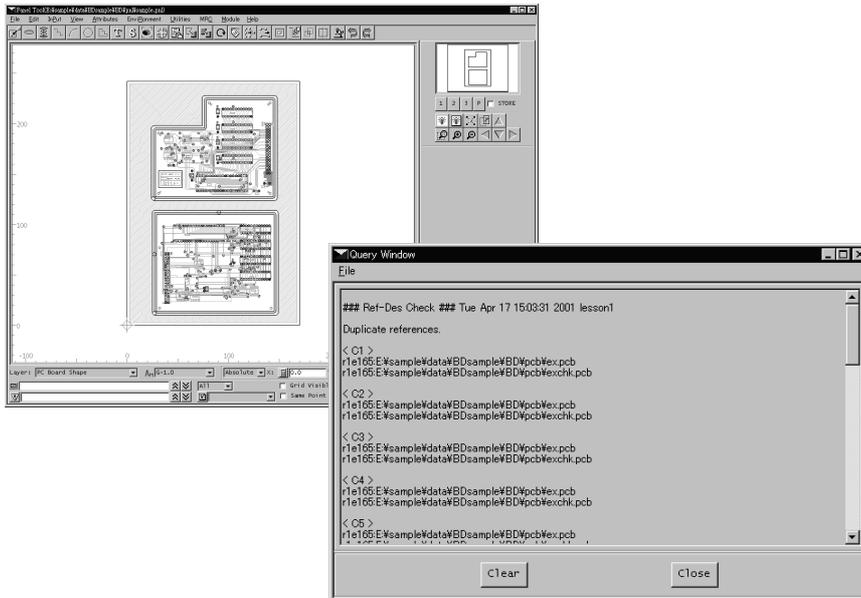
## ● Reference overlap check

### [Function]

You can check if references for the components on PC boards placed on the panel and with different file paths overlap each other.

### [Operation]

- (1) Click **MRC** → **Reference Overlap Check** from the menu bar.



### [Notes and Restrictions]

- This check does not cover panel components and PC boards with the same file path.

## ● PC board input reversion function made an option

### [Function]

The PC board input reversion function is now an option for Rev. 6.0.

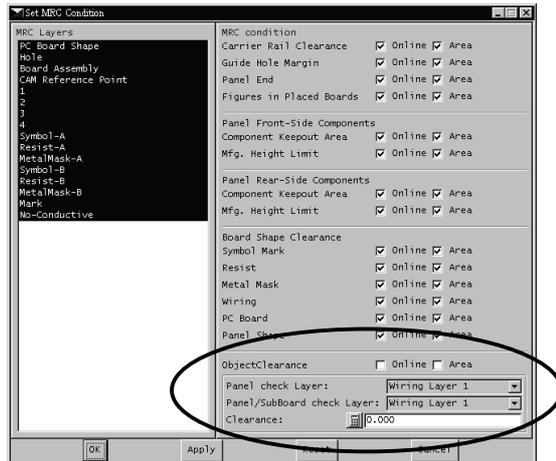
If you are using the Rev. 5.0 Manufacturing Panel Design Tool, you can this option as usual.

## 6-2 Enhanced MRC Function



### [Function]

The Manufacturing Panel Design Tool can check clearance between a panel object and one on the placement PC board with the MRC function. The tool can also check clearance between panel objects. This enables the checking of manufacturing problems such as a adversely effected PC board foil and components caused by stress occurring when a PC board is torn from a panel along perforation.



### [Notes and Restrictions]

- Objects on the drawing layer and production reference points are not checked.
- Clearance between objects on the placement PC board are not checked.
- Layers not set to visible layers are checked.
- Online MRC does not check clearance to an object on the PC board at PC board input.
- If in-component objects on the panel are specified as check area, Area MRC checks not only objects in the area but also all objects on the component's check target layer.

# 6-3 Editing Manufacturing Rule

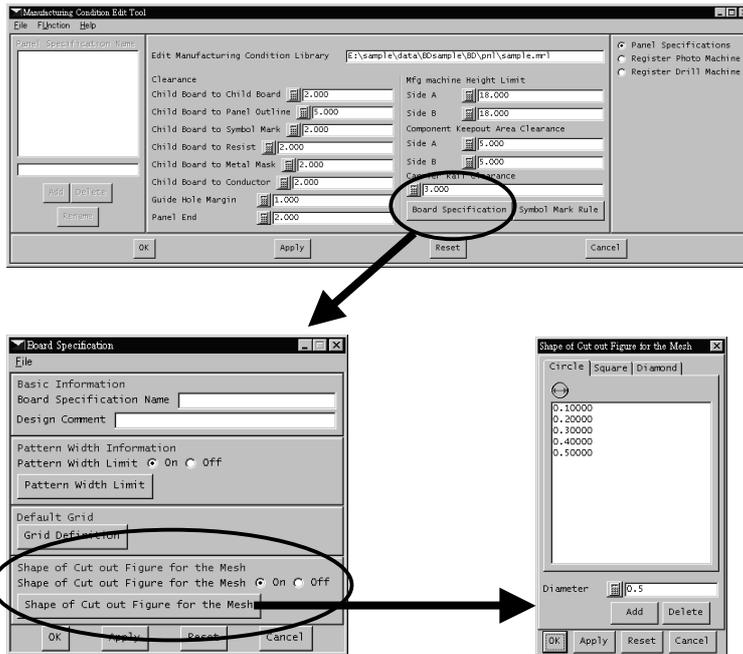


## [Function]

With Rev. 5.0, you can freely specify any mesh size during panel design for mesh plane generation.

With Rev. 6.0, you can set the mesh size limit as a manufacturing rule.

This avoids cutout figures with inappropriate mesh size for production.



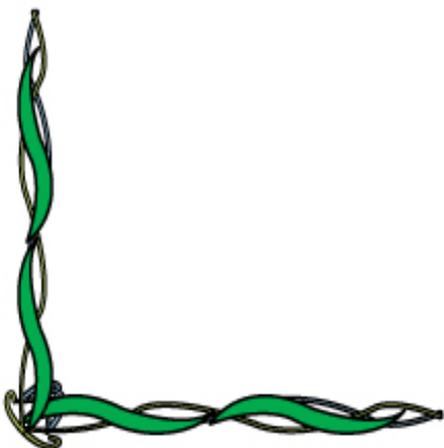
## [Notes and Restrictions]

- PC board specifications for manufacturing rules are copied from the design rule library when the panel database is created. Consequently, the mesh cutout figure limit is specified as a local manufacturing rule.



# Chapter 7

## CAM



# 7-1 Photo Output Program



The following functions are added or improved for the Photo Data Output Program.

- NC format information added to the photo data list
- Improved character mirroring

## ● NC format information added to the photo data list

### [Function]

The output photo data list includes NC format information referred to at output from the manufacturing rule library (MRDB) upon photo output.

The following items related to the NC format set in the MRDB are output for Rev. 6.0.

- Character Code
- Record Format
- Record Length
- NC Data Unit
- Coordinate Format
- Coordinate Representation
- Omit Coordinates
- Zero Suppress
- EOB Code
- EOR Code
- ETB Code
- PAD Code

```

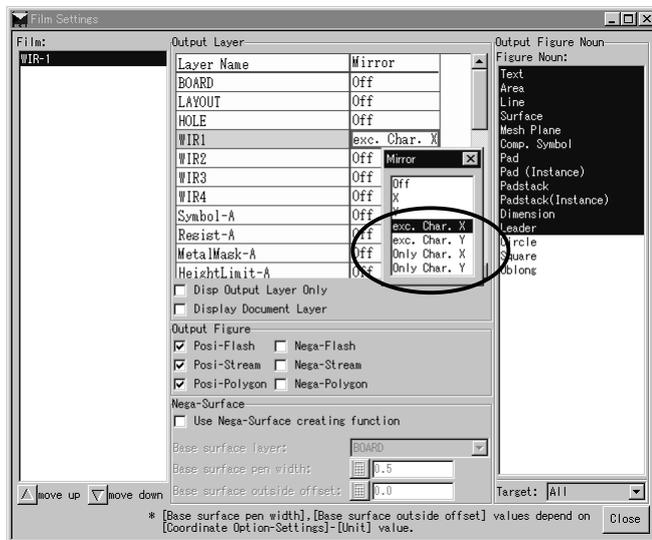
***** PHOTO DATA LIST *****
Date/Time : Wed Apr 18 11:48:14 2001
Host Name : "r1e1s4"
Directory : "d:\home\lesson2"
User Name : lesson2
<PHP> File : "C:\TEMP\Param8.php"
Comment : ""
<PML/PCB> File : "r1e1s4:C:\home\lesson2\pcb\ex.pcb"
<NRL/MRDB> File : "C:\home\lesson2\mrdb\zuken.mrdb"
Photo Machine : "ZUKEN_photo"
Character Code : ASCII
Record Format : Full Storage
Record Length : 512
NC Data Unit : Millimeters
Coordinate Format : 000.000
Coordinate Representation : Absolute
Omit Coordinates : Off
Zero Suppress : Leading Zero Suppress
EOB Code : LF
EOR Code : SPACE
ETB Code : SPACE
PAD Code : SPACE
<PHD> File : "C:\home\lesson2\pcb\test.phd"
<PHP> File : "C:\home\lesson2\pcb\test.ph"
List Unit : Millimeters
Layer(Drawings)-(Mirror) : Symbol-A(without) - ( off)
Noun Name : TEXT
AREA
LINE
SURF
SYMBOL
PADREF
PADINST
PADSTKREF
PADSTKINST
DIMLEADER
MESHPLANE
Flare : POSI ([F] [S] [P])
Rotation : ( 0)
Origin : ( 0.000, 0.000)
Scale : ( 1.000)
Offset : ( 0.000, 0.000)
Aperture Table :
-----
| No | D-CODE | TYPE | FIG | DIM/W | IN-DIM/H | ANGLE | SLIT W | SLIT COUNT | PAD NAME |
-----
| 1 | D119 | STRM | CI | 0.200000 | | | | | |
-----
* FLSH = POSI FLASH STRM = POSI STREAM PGON = POSI POLYGON
N-FLSH = NEGA FLASH N-STRM = NEGA STREAM N-PGON = NEGA POLYGON
** CI = CIRCLE SQ = SQUARE RE = RECTANGLE DO = DONUT
RT = ROUND_THERMAL ST = SQUARE_THERMAL CU = CUSTOM(ODD_SHAPE)
Aperture Count :
-----
| No | D-CODE | FLASH | STREAM | POLYGON | N-FLASH | N-STREAM | N-POLYGON | MOVE DIST. | DRAW DIST. |
-----
| 1 | D119 | 0 | 33 | 0 | 0 | 0 | 0 | 878.853 | 896.718 |
-----
| Total | | 0 | 33 | 0 | 0 | 0 | 0 | 878.853 | 896.718 |
-----
Data Area : ( 7.000000, 6.820000) - (115.670000, 87.630000)
    
```

## ● Improved character mirroring

### [Function]

With Rev. 5.0, character mirroring is performed in the X- or Y-direction on the display.

With Rev. 6.0, X-mirroring is performed based on the line horizontal to characters and Y-mirroring is performed based on the line vertical to characters. This improvement solves problems such as the silk pattern overlapping a component pin. This mirroring is performed when the mirror mode is “character exclusion” or “character only.”



### [Notes and Restrictions]

- Processing in the “X-direction” and “Y-direction” mirror modes has not been changed.

### Reference

For examples of character mirroring, see “1-9 Plotting PC board ●Improved character mirroring.”

# 7-2 Photo Tool



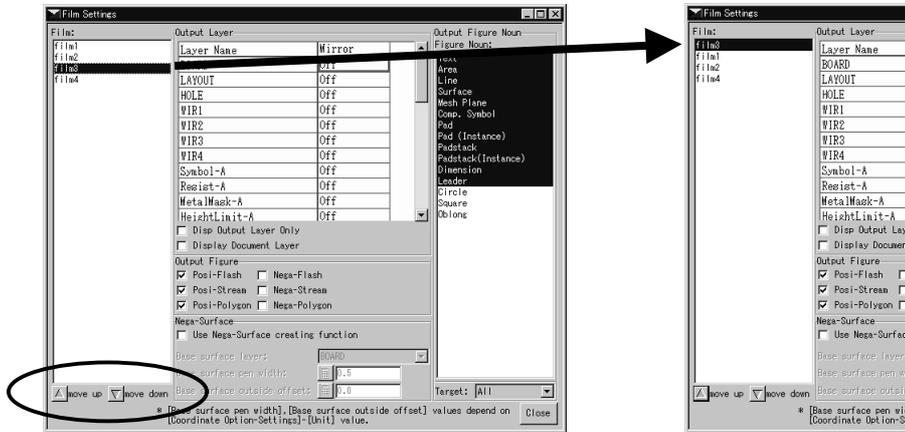
The following functions are added or improved for the Photo Data Output Tool.

- Function added to specify the output order
- Function added to output files with the post program

## ● Function added to specify the output order

### [Function]

When multiple films are set, the Photo Data Output Tool outputs photos in the order that they are set, but you can change the outputting order.

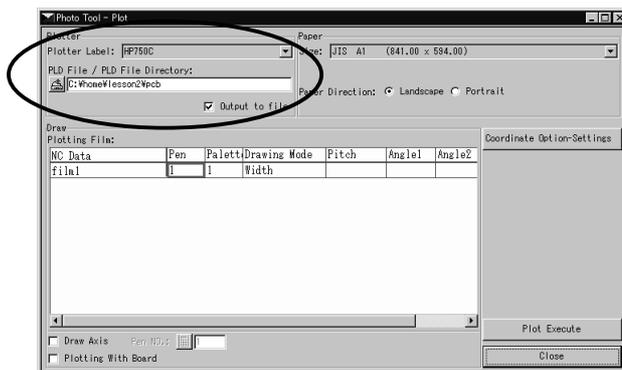


## ● Function added to output files with the post program

### [Function]

Rev. 5.0 can output photo plotting data to files in only four formats: “CR-5000,” “CR-3000,” “HP- GL” and “LIPS.”

With Rev. 6.0, you can output data to other post programs. This enables data output that has been directly output to the plotter or printer as a plotting intermediate file.



# 7-3 Drill Output



The following functions are added or improved for the Drill Data Output Program.

- NC format information added to the drill data list
- Increased hole-type numbers
- Expanded oblong hole output function

## ● NC format information added to the drill data list

### [Function]

The output drill data list includes NC format information referred to at output from the manufacturing rule library (MRDB) upon drill output.

The following items related to NC format set in the MRDB are output for Rev. 6.0.

- Character Code
- Record Format
- Record Length
- NC Data Unit
- Coordinate Format
- Coordinate Representation
- Omit Coordinates
- Zero Suppress
- EOB Code
- EOR Code
- ETB Code
- PAD Code

```
***** DRILL DATA LIST *****
Date/Time : Wed Apr 18 13:06:33 2001
Host Name : "r1e184"
Directory : "d:\home\lesson2"
User Name : lesson2

<PDL/PCB> File : "r1e184\C:\home\lesson2\pcb\yev.pcb"
<MRL/MRDB> File : "C:\home\lesson2\mrdb\zuken.mrdb"
Drill Machine : "ZUKEN_drill"

Character Code : ASCII
Record Format : Full Storage
Record Length : 612
NC Data Unit : Millimeters
Coordinate Format : 000.00
Coordinate Representation : Incremental
Omit Coordinates : Off
Zero Suppress : Leading Zero Suppress
EOB Code : LF
EOR Code : SPACE
ETB Code : SPACE
PAD Code : SPACE

<DRD> File : "C:\home\lesson2\pcb\drill1.drd"
<DRL> File : "C:\home\lesson2\pcb\drill1.drl"

List Unit : Millimeters
Origin : (0.000 ,0.000)
Mirror : OFF
Rotation : ( 0 )
Scale : (1.000)
Offset : (0.000 ,0.000)

Drill Data :
+-----+-----+-----+-----+-----+-----+-----+-----+
| No. | T_code | Kind | Shape | Size | Type | Hits | Move | MAX(X,Y) |
+-----+-----+-----+-----+-----+-----+-----+-----+
| 1 | T01 | Normal | Circle | 0.600 | 0 | 62 | 1088.788 | 1000.100 |
+-----+-----+-----+-----+-----+-----+-----+-----+
| 2 | T02 | Normal | Circle | 0.700 | 0 | 182 | 990.269 | 952.810 |
+-----+-----+-----+-----+-----+-----+-----+-----+
| 3 | T03 | Normal | Circle | 2.000 | 0 | 5 | 385.242 | 366.760 |
+-----+-----+-----+-----+-----+-----+-----+-----+
| Total | | | | | | 249 | 2474.297 | 2319.670 |
+-----+-----+-----+-----+-----+-----+-----+-----+

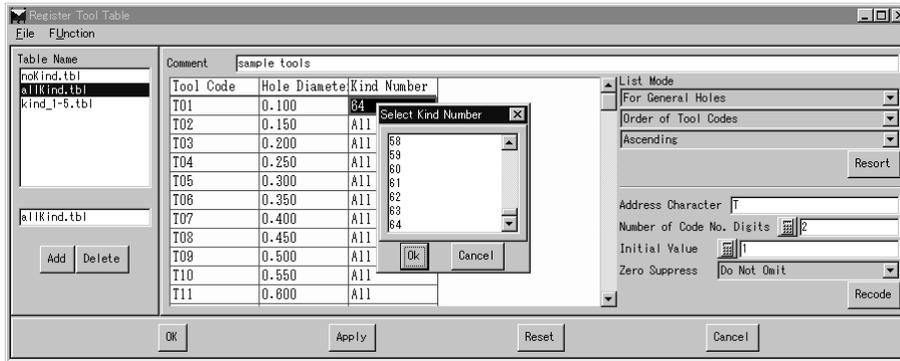
Data Area : (5.000 ,5.000)-(115.000 ,95.000)
```

## ● Increased hole-type numbers

### [Function]

With Rev. 5.0, the range of hole-type number is 0 to 15.

With Rev. 6.0, you can set a number between 0 to 64. The settable range of hole-type numbers in the manufacturing rule library, which is referred to at drill output, are accordingly changed to the 0 to 64 range.

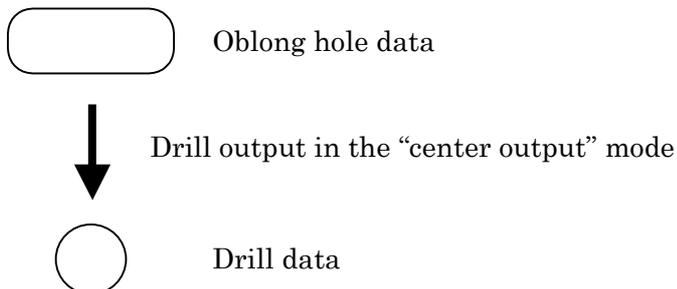


## ● Expanded oblong hole output function

### [Function]

With Rev. 5.0, there are three modes for oblong hole output: “alternate output from the ends,” “output from an end” and “three-point output.”

With Rev. 6.0, the “center output” mode is added. In this mode, drill output is performed for oblong hole center.



# 7-4 Drill Tool



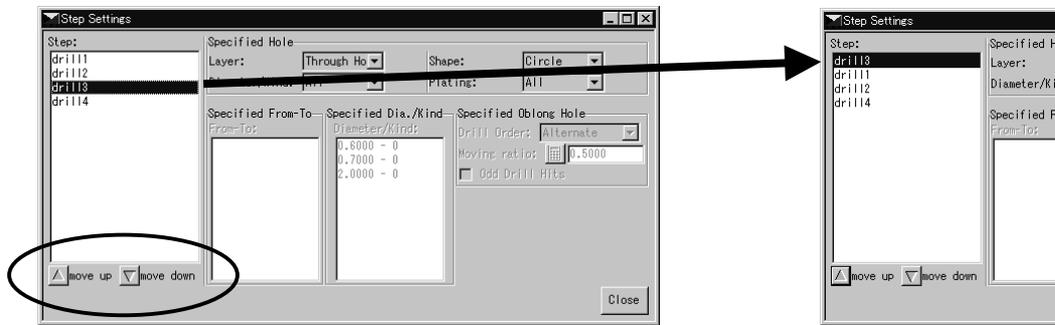
The following functions are added or improved for the Drill Data Output Tool.

- Function added to specify the output order
- Function added to output files with the post program

## ● Function added to specify the output order

### [Function]

When multiple output drill phases are set, the Drill Data Output Tool performs drilling in the order that they are set, but you can freely change the output drill phase order.

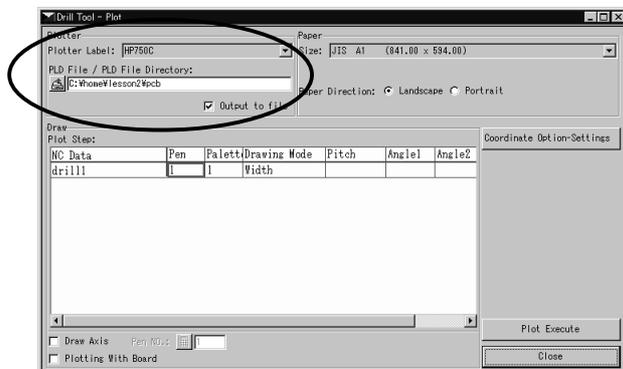


## ● Function added to output files with the post program

### [Function]

Rev. 5.0 can output drill plotting data to files in only four formats: “CR-5000,” “CR-3000,” “HP- GL” and “LIPS.”

With Rev. 6.0, you can output data to other post programs. This enables data output that has been directly output to the plotter or printer as a plotting intermediate file.



---

# 7-5 CAM Information List Output Program

---



Rev. 6.0 has the following new functions.

- Specifying the range of the output angle
- Expressing the angle from the viewpoint of the specified-side

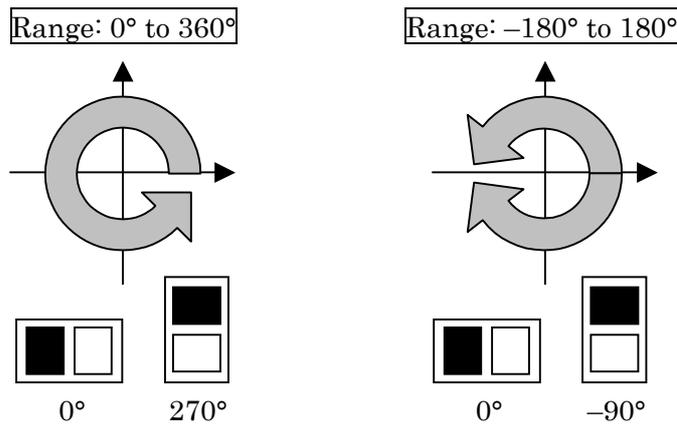
## ● Specifying the range of the output angle

### [Function]

With Rev. 5.0, the angle is output within the range of  $0^\circ$  to  $360^\circ$ .

The mode to output the angle from  $-180^\circ$  to  $180^\circ$  is added for Rev. 6.0.

Normally, the X-axis direction is regarded as  $0^\circ$  and the angle is output counterclockwise. When the  $-180^\circ$  to  $180^\circ$  output range is specified, the conventional  $180^\circ$  to  $360^\circ$  range is output as negative value clockwise.



### [Operation]

You need a parameter file to execute this function. Prepare it by using the `-p:mkparam` option or by other means.

If you set 2 to the angle range in the corresponding item (AngleMode) in the parameter file, you can output an angle from  $-180^\circ$  to  $180^\circ$ .

AngleMode: [Angle range]: [Side-view mode]

[Angle range]

Select one of the following two.

- 1 : The output range is  $0^\circ$  to  $360^\circ$ .
- 2 : The output range is  $-180^\circ$  to  $180^\circ$ .

When this is omitted, the output range is  $0^\circ$  to  $360^\circ$ . (The default is “1.”)

## ● Expressing the angle from the viewpoint of the specified-side

### [Function]

With Rev. 5.0, the component angle for A-side components is output from the A-side view and that for B-side components is from the B-side view.

With Rev. 6.0, you can output the angle as shown with the request command on the tool (all components A-side view angle) or output an angle for all components from the B-side view.

### [Operation]

You need a parameter file to execute this function. Prepare it by using the `-p:mkparam` option or by other means.

Set a side-view mode in the corresponding item (AngleMode) in the parameter file.

AngleMode: [Angle range]: [Side-view mode]

[Side-view mode]

Select one of the following three.

Default: A-side components are output with the A-side view angle and B-side components are output with the B-side view angle.

CAD-A: Outputs all components with the A-side view angle. (Same as output by the request command)

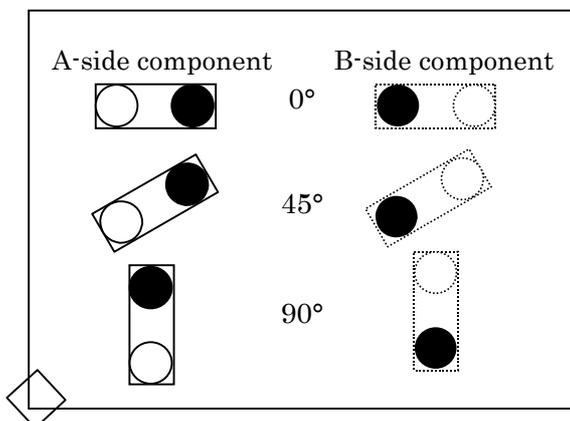
CAD-B: Outputs all components with the B-side view angle.

When omitted: A-side components are output with the A-side view angle and B-side components are output with the B-side view angle.  
(Same as specifying "Default.")

Angle output in the [side-view mode] is as follows.

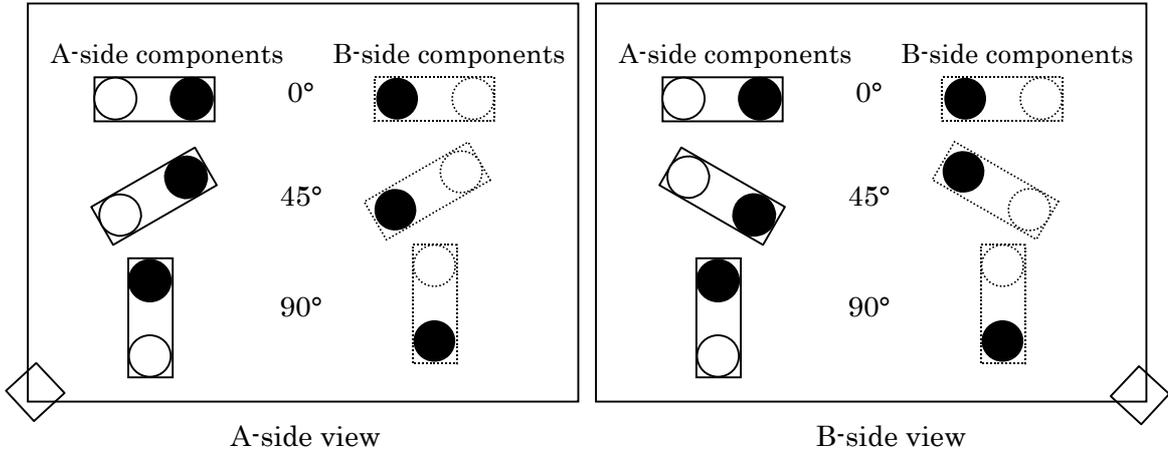
([Angle range] is from 0° to 360°.)

Component angle output with the request command



**<Output when Default is specified>**

Request angle	A-side 0°	A-side 45°	A-side 90°	B-side 0°	B-side 45°	B-side 90°
Output angle	0°	45°	90°	0°	315°	270°



**<Output when CAD-A is specified>**

Request angle	A-side 0°	A-side 45°	A-side 90°	B-side 0°	B-side 45°	B-side 90°
Output angle	0°	45°	90°	0°	45°	90°

**<Output when CAD-B is specified>**

Request angle	A-side 0°	A-side 45°	A-side 90°	B-side 0°	B-side 45°	B-side 90°
Output angle	0°	315°	270°	0°	315°	270°

**[Notes and Restrictions]**

- The angle calculation in the [side-view mode] is valid only for the component angle and does not affect the angles of the PC board and holes.

# 7-6 CAM Check Tool

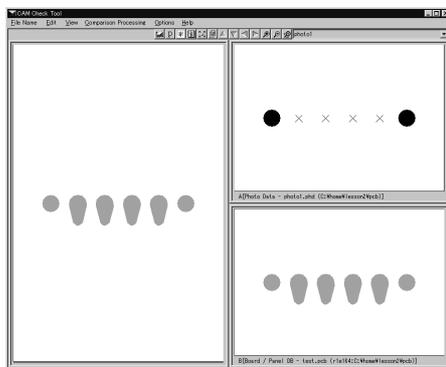


## [Function]

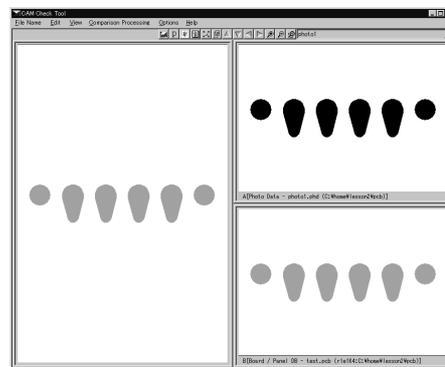
With Rev. 5.0, you cannot acquire shape information from photo data with different apertures because it can only check correspondence between D-codes and pad names. Therefore, when the CAM Check Tool displays different aperture data on the screen, only × mark is displayed to indicate the output position of flash data.

Rev. 6.0 can compare different aperture shapes output as flash by referring to the PCB database (PCB) and panel database (PNL). This enables display of a different aperture as a different shape on the screen.

Rev.5.0

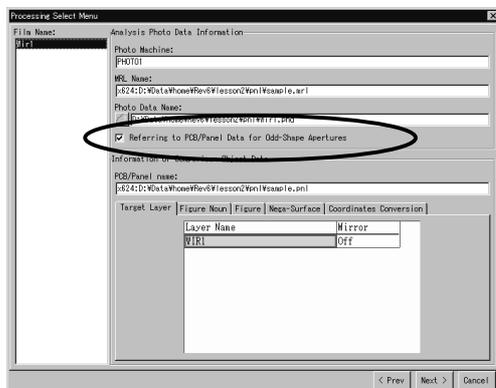


Rev.6.0



## [Operation]

- (1) Start the CAM Check Tool and then select **File**→**New** from the menu bar.
- (2) Select “Photo data PC board/panel data comparison” from the process selecting menu.
- (3) Select “parameters at the time of photo output are saved” or “only photo data is saved” depending on whether the parameter file exists, and then input a filename.
- (4) Select the “Referring to PCB/Panel Data for Odd-Shape Apertures” check box under Analysis Photo Data Information.



- (5) Click **Next** and set by following the directions for the Wizard.

---

# 7-7 In-circuit Tester Output Program

## [Optional]

---



### [Function]

Rev. 6.0 has a new resource file (tpprobe.rsc) referred to upon automatic test point extraction by BD. The In-circuit Tester Output Program can output information such as tool Nos. and probe pins by referring to this resource file, enabling the user to share and output information set on the CAD.

```
#####  
#Pitch Rank Priority  
#####  
#ex)  
# PitchPrio 2{  
#   priority "pitchRankId:pitch"  
# }  
#  
#   priority      : 1 ~n integer "Priority"  
#   pitchRankId  : string "Pitch Rank ID"(see ProbeTbl &ProbePrio section)  
#   pitch        : float "Pitch value"  
#  
#                   (priority1 pitch >priority2 pitch >...)  
#   toolNo: string "Tool No.use ictout"  
#####  
PitchPrio 2{  
  1   "Pitch1   : 2.54: T03"  
  2   "Pitch2   : 1.78: T02"  
  3   "Pitch3   : 1.27: T01"  
}  
↑ ↑ ↑ ↑  
Priority Pitch rank ID Pitch diameter Tool No.
```

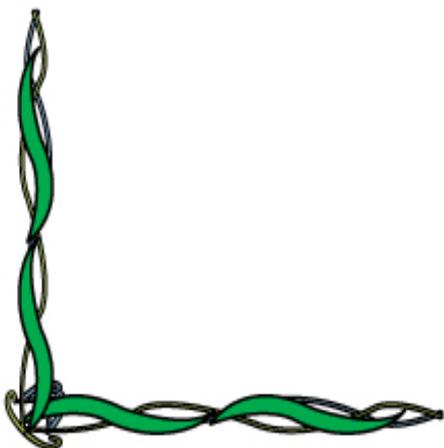
### [Notes and Restrictions]

- Rev. 6.0 does not support Tool Nos., which are conventionally set in the “Tool No.” section in the parameter file (XXX.iop). Rev. 6.0 ignores such a setting in the parameter file (though this does not cause an error).

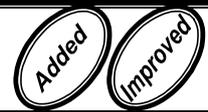


# Chapter 8

## Other Tools



# 8-1 PWS Translator



## [Function]

The following conversion modes are added or improved.

- Added function common to each conversion mode
- Added function common to each BD-to-PWS conversion mode
- Added function for NCF-to-MRDB conversion
- Conversion specification parameters
- Parameter convertibility
- Notes and restrictions on operation

## ● Added function common to each conversion mode

The following functions are added or improved for Rev. 6.0.

- User font support
- Component X-axis reversion support

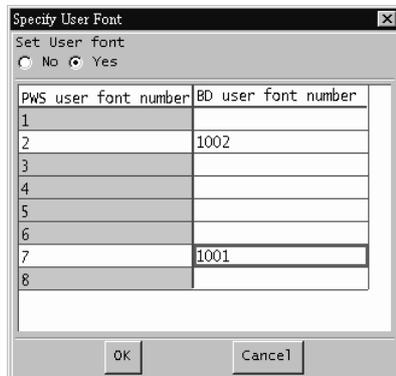
## User font support

### [Function]

In line with user font support, you can convert the user font numbers between PWS and BD when they are used by a character, component symbol or dimension line text.

### [Operation]

- (1) Click **Conversion Way** from the parameter setting items.
- (2) Select **Function** → **Set User Font** from the menu bar.
- (3) Set **[Yes]** to **[Set User Font]** and specify the corresponding font number.
- (4) Click **OK**.



The dialog box titled "Specify User Font" has a close button (X) in the top right corner. Below the title bar, it says "Set User font" and has two radio buttons: "No" (unselected) and "Yes" (selected). Below this is a table with two columns: "PWS user font number" and "BD user font number". The table has 8 rows. Row 1: PWS=1, BD=1. Row 2: PWS=2, BD=1002. Row 3: PWS=3, BD=1. Row 4: PWS=4, BD=1. Row 5: PWS=5, BD=1. Row 6: PWS=6, BD=1. Row 7: PWS=7, BD=1001. Row 8: PWS=8, BD=1. At the bottom of the dialog are "OK" and "Cancel" buttons.

PWS user font number	BD user font number
1	1
2	1002
3	1
4	1
5	1
6	1
7	1001
8	1

## Reference

To convert user font data, see “1-13 User Font ●PWS user font conversion.”

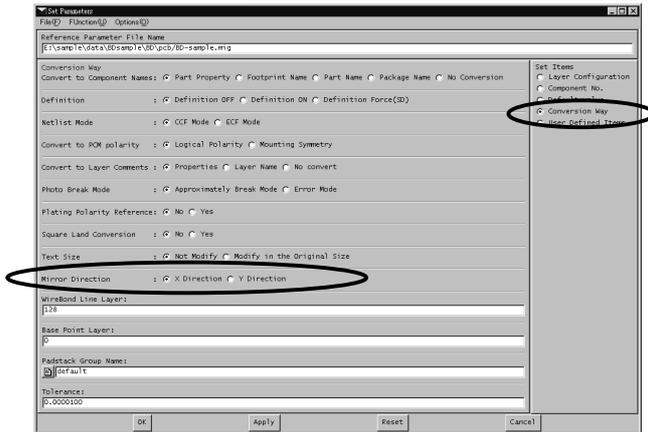
## Component X-axis reversion support

### [Function]

To use the B-side component registered in the Y-direction (X-axis reversion) on PWS, you can specify the Y-direction (X-axis reversion) upon PWS-to-BD and BD-to-PWS conversion with Rev. 6.0.

### [Operation]

- (1) Click **Conversion Way** from the parameter setting items.
- (2) Specify the **Y-direction (X-axis reversion)** for [Mirror Direction].



### [Notes and Restrictions]

- When the Y-direction (X-axis reversion) is specified, character data registered as PWS B-side component is registered mirrored in the Y-direction on CDB.

## ● Added function common to each BD-to-PWS conversion mode

### [Function]

The following functions are added or improved for Rev. 6.0.

- Function to convert to square land
- Improved pin shape priority

## Function to convert to square land

### [Function]

With Rev. 6.0, you can convert a square surface pad with the BD or CDB flash attribute into a PWS square land.

## Improved pin shape priority

### [Function]

When the component pin has 1 pin and multiple shapes in both the PCB and component files, the conversion priority is improved: Padstack with hole > padstack without hole > pad > others (line, surface).

## ● Added function for NCF-to-MRDB conversion

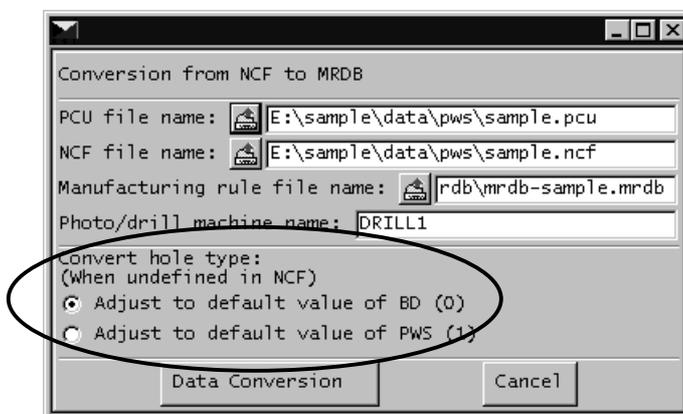
### [Function]

With Rev. 5.0, when the drill type is undefined (value: 1) on NCF for PWS drill, “1” is set to the hole type upon conversion to MRDB.

With Rev. 6.0, you can select “PWS default: 1” or “BD default: 0.”

### [Operation]

- (1) Select **Function** → **NCF→MRDB Conversion** from the PWS translator menu bar.
- (2) Select [Adjust to default value of BD (0)] or [Adjust to default value of PWS (1)] in the dialog box.
- (3) Click **Data Conversion**.



## ● Conversion specification parameters

### [Function]

Parameters set for conversion specification on the parameter setting menu of each tool are added in Rev. 6.0.

Conversion specification parameters settable on Rev. 5.0 tools and parameters newly added on Rev. 6.0 are listed below.

### Parameters referred to upon PWS-to-CDB or -BD conversion

○: Referred to on Rev. 5.0 or older   ◆: Rev. 6.0: Added for reference on Rev. 6.0   ×: Not referred to

	PWS to BD	PWS to CDB/BD	PWS to BD	PWS to BD
	Library conversion	PC board conversion	PC board conversion	Artwork conversion
Net list (NDF) reference	×	○	×	×
Conversion to pin number	○	○	×	×
Changing pin reference point	○	×	×	×
Merging pin shapes	○	○	○	○
Conversion shape of surface component pin	○	○	○	○
CDB creation	○	○	×	×
Changing component shape on PC board	×	○	○	○
Character data size	○	○	○	○
Vector font name	○	○	○	○
Target layer for wire-bonding connection data search	○	○	×	×
Hole input layer not to be converted	○	○	○	○
Padstack group name	○	○	○	○
Wiring information conversion	×	×	○	×
Deleting existing wiring layer data	×	×	○	×
Placement information conversion	×	×	○	○
Component reversion direction	◆	◆	◆	◆
User font specification	◆	◆	◆	◆

\* Parameters added to Rev. 6.0 are hatched.

<Parameter added for Rev. 6.0>

#### ● Component reversion direction

You can select the component reversion direction.

#### ● User font specification

You can specify the user font number for data to convert and data created after conversion.

\*For parameters used on Rev. 5.0 or older, see the User's Guide or online help.

## Parameters referred to on CDB- or BD-to-PWS conversion

○: Referred to on Rev. 5.0 or older   ◆: Rev. 6.0: Added for reference on Rev. 6.0   ×: Not referred to

	CDB to PWS	BD to PWS	BD to PWS	BD to PWS	BD to PWS
	Library conversion	PC board conversion	Artwork conversion	Component conversion	Placement /wiring conversion
Conversion to component name	○	○	○	○	×
Component creation	○	×	×	×	×
Element allocation	○	○	×	○	×
Net format	×	○	×	×	×
Conversion PCM polarity	○	○	○	○	×
Conversion to layer comment	○	○	○	○	×
Photo expansion mode	○	○	○	○	○
Plating attribute reference	○	○	○	○	○
Component shape on PC board	×	×	×	×	○
Character data size	○	○	○	○	○
Wire-bonding line output layer	○	○	○	○	×
Mounting reference point output layer	○	○	○	○	×
Padstack group name	○	○	○	○	○
Tolerance	○	○	○	○	○
Conversion to square land	◆	◆	◆	◆	◆
Component reversion direction	◆	◆	◆	◆	◆
User font specification	◆	◆	◆	◆	◆

\* Parameters added for Rev. 6.0 are hatched.

<Parameter added for Rev. 6.0>

● Conversion to land

You can specify whether to convert a square surface pad with the flash attribute to PWS square land.

● Component reversion direction

You can select a component reversion direction.

● User font specification

You can specify the user font number for data to convert and data created after conversion.

\*For parameters used on Rev. 5.0 or older, see the User's Guide or online help.

## ● Parameter convertibility

### Parameter convertibility between Rev. 5.0 and Rev. 6.0

You can use Rev. 5.0 parameter files as they are on Rev. 6.0. (You can use the parameter file created for Rev. 6.0 on Rev. 5.0.)

In this case, default is set to all added items.

The default for parameters added for Rev. 6.0 conversion are as follows.

- Library conversion from PWS-to-CDB
- PC board conversion from PWS-to-CDB/BD
- PC board conversion from PWS-to-BD
- Artwork conversion from PWS-to-BD

Conversion specification parameter

Component reversion direction : X-direction (Y-axis reversion)

User font specification : not specified (the user font is not converted.)

- Library conversion from CDB-to-PWS
- PC board conversion from BD-to-PWS
- Artwork conversion from BD-to-PWS
- Component conversion from BD-to-PWS
- Placement wiring conversion from BD-to-PWS

Conversion specification parameter

Conversion to square land : not specified

Component reversion direction : X-direction (Y-axis reversion)

User font specification : not specified (the user font is not converted.)

### Using parameters on Rev. 6.0

The same item can be referred to at conversion in both directions. We recommend creating different parameter files for each conversion direction and conversion mode.

## ● Notes and restrictions on operation

Rev. 6.0 supports PWS database Rev11.0 or newer.

---

## 8-2 Root Editor Interface [Optional]

---



### [Function]

With Rev. 5.0, wiring is lock per net.

With Rev. 6.0, wiring is locked per wiring or Via

### Reference

For lock attributes, see “4-14 Set Net Display Color Dialog Box • Deleted lock attribute item.”

---

## 8-3 SPECCTRA Interface [Optional]

---



### [Function]

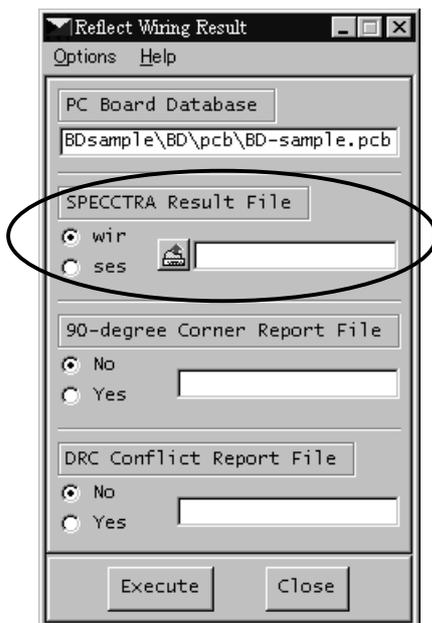
The following functions are added or improved for Rev. 6.0.

- Specifying the SPECCTRA result filename
- Changed wiring lock unit

### ● Specifying the SPECCTRA result filename

### [Function]

You can specify a filename for “wir” or “ses” when returning placement/wiring results to BD.



### ● Changed wiring lock unit

### [Function]

With Rev. 5.0, wiring is locked per net.

With Rev. 6.0, wiring is locked per wiring or Via

### Reference

For the lock attribute, see “4-14 Set Net Display Color Dialog Box • Deleted lock attribute item.”

# 8-4 Post-layout Analysis Interface [Optional]



The following functions are added or improved.

- ICX interface [Optional]
- XTK/QUIET interface [Optional]
- SPECCTRAQuest interface [Optional]
- SMM interface [Optional]
- Apsim interface [Optional]

The following tools are added.

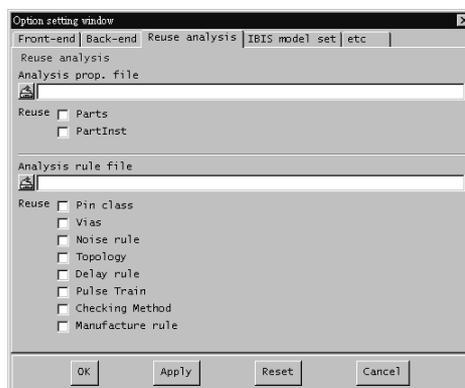
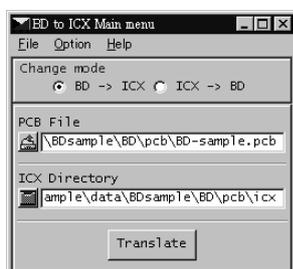
- Hot-Stage interface [Optional]
- TPA interface [Optional]
- HFSS/Spicelink interface [Optional]

## ● ICX interface [Optional]

### [Function]

The following functions are added or improved for Rev. 6.0.

- Direct output of NDD file (ASCII file for ICX)
- Added data to transfer to ICX
- Adopted new option setup window



## ● XTK/QUIET interface [Optional]

### [Function]

The following functions are added or improved for Rev. 6.0.

- Creating an appropriate model (for which the number of pins conforms to the IO attribute)
- Added select net zoom button
- Electrical net selection support
- File with an arbitrary extension can be a transmission line model search target
- Outputting “ALLOW\_PIN\_OVERLAPS=TRUE” to the GCF file
- Sorting and listing the model names in the Model selection dialog box

## ● SPECCTRAQuest interface [Optional]

### [Function]

The following functions are added or improved for Rev. 6.0.

- Making prohibited characters (to be converted to “\_” by the interface) the same as the SPECCTRAQuest I/F for System Designer
- Specifying the part attribute name defining the component constant for Environmental Variable “BD2SQVAL”
- Drawing lines in pad or padstack

## ● SMM interface [Optional]

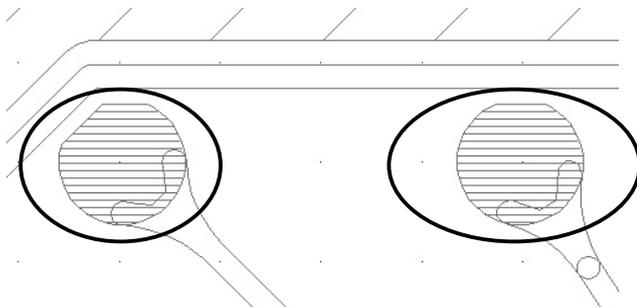
### [Function]

This interface now supports Hot-Stage.

## ● Apsim interface [Optional]

### [Function]

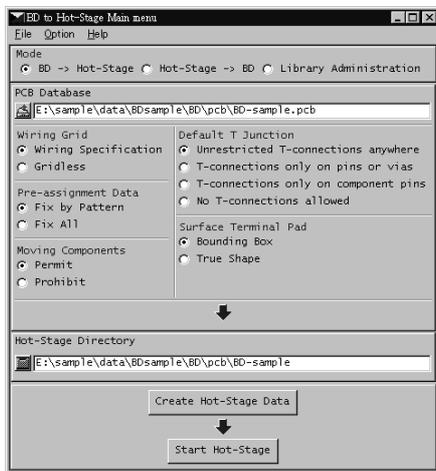
With Rev. 6.0, this interface can output an actual shape of a pad even if the pad shape is not “circular” nor “rectangle.”



## ● Hot-Stage interface [Optional]

### [Function]

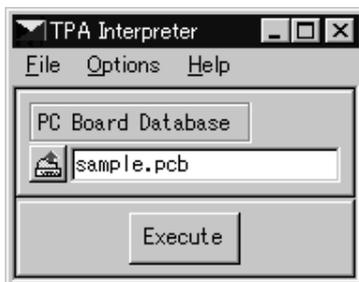
An interface function has been developed for Hot-Stage.



## ● TPA interface [Optional]

### [Function]

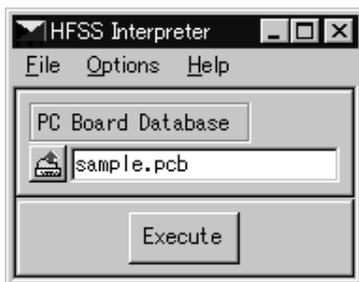
An interface function has been developed for Ansoft's package structure characteristic extraction program, TPA (Turbo Package Analyzer).



## ● HFSS/Spicelink interface [Optional]

### [Function]

An interface function has been developed for Ansoft's 3-D high-frequency electromagnetic field simulator, HFSS/Spicelink.

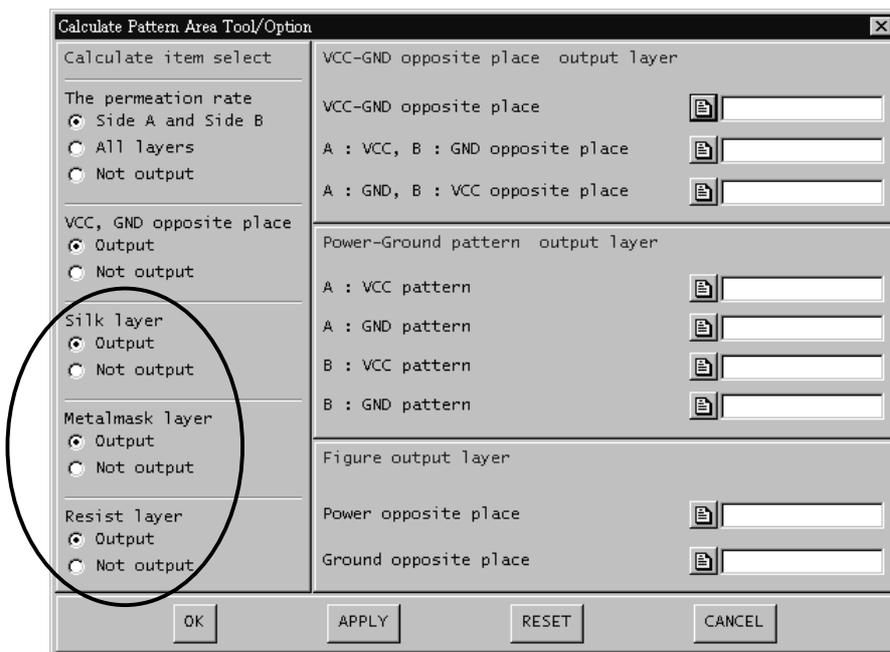


# 8-5 Calculate Pattern Area Tool [Optional]



## [Function]

With Rev. 6.0, you can output the area of the Silk, Metalmask and Resist layers.



## Output example

```
=====Silk layer=====
Symbol-A: 378.204
Symbol-A-1: 53.195
Symbol-B: 218.546
Symbol-B-1: 31.325

=====Metalmask layer=====
MetalMask-A: 492.880
MetalMask-B: 287.230

=====Resist layer=====
Resist-A: 8565.524
Resist-B: 8569.913
```

---

# 8-6 CR-5000 Object-Oriented DB Access Class Library (ZFC)

---



## [Function]

With Rev. 6.0, you can access the following information in addition to the conventional editing range.

New arithmetic operation functions such as surface and character outline extraction calculation are added.

- Character size table information (parameter container)
- Net list information (design rule container)
- Decoupling capacitor and jumper component information (design rule container)
- Square hole type number (figure/footprint container)

## Supported OS and compiler

To create application with ZFC on Rev. 6.0, the following compilers are required.

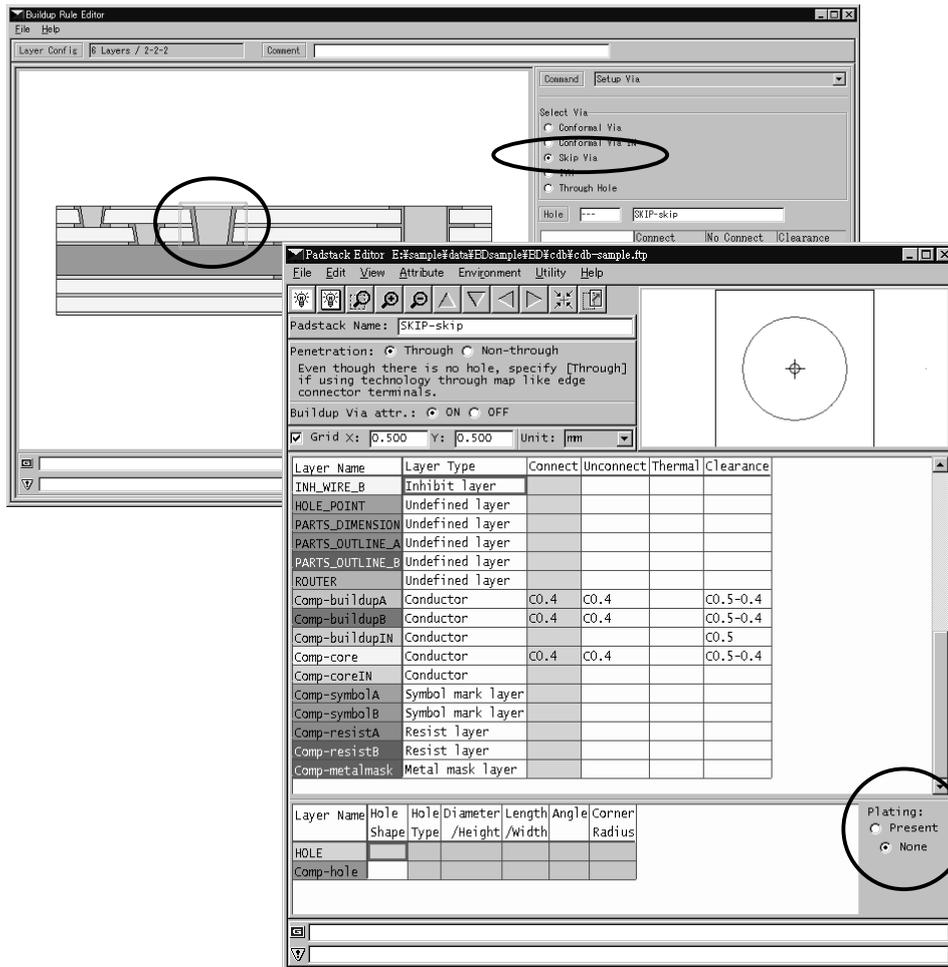
Platform	OS version	Compiler
HP	HP- UX B.10.20	HP ANSI C++B3910B A.01.15 or upper
SUN	Solaris.2.5.1/2.6/7	SUN WorkShop Compilers 4.2.1 C++ SUN WorkShop Compilers 5.0 C++ (should be used in the compt mode)
	Solaris.2.6/7	SUN Forte C++6.0 (should be used in the compt mode)
PC	WindowsNT4.0 SP5 or upper	Microsoft Visual C++6.0 Professional Edition SP3 or upper
	Windows2000 SP1 or upper	

# 8-7 Build-Up Basic Module [Optional]



## [Function]

The Build-up Design Rule Editor registers “Skip Via” without plating attribute to CDB.



## Reference

For Skip Via and net connection, see “4-16 Padstack Plating Attribute Support • Net connection calculation.”

## 8-8 3D viewer [Optional]



### [Function]

The following functions are added or improved for the 3D viewer.

- Added view operation icons
- Function added to display non-connected net and pin numbers
- Added query function

### ● Added view operation icons

### [Function]

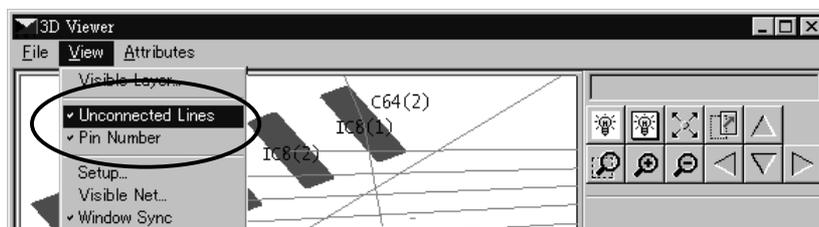
Icons for view operations such as zoom, pan, display all, re-display are added.



### ● Function added to display non-connected net and pin numbers

### [Function]

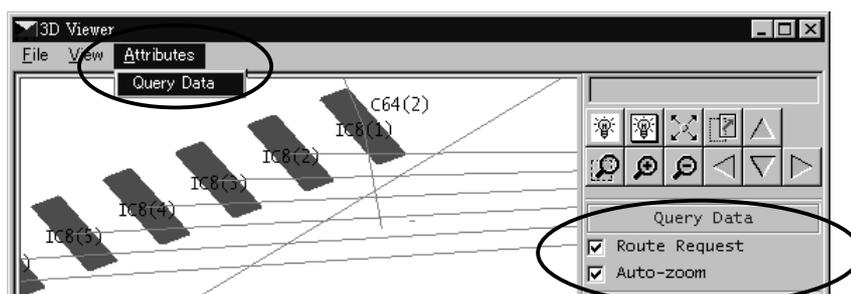
You can turn non-connected net and pin number displays on/off.



### ● Added query function

### [Function]

The query function is added to acquire information necessary for high-speed schematic designing on the 3D viewer for Rev. 6.0.



# 8-9 Package Basic Module [Optional]



## [Function]

The following functions are added or improved to design the inside of the high-density LSI package (Advanced Package).

The image displays several key features of the software's bond shell and package design capabilities:

- Bond shell generation program:** A 2D schematic showing the layout of a bond shell with labels for Wire-bonding pad, Powering, Bonding-wire, and Ground ring.
- 3-D bond shell viewer:** A 3D perspective view of the bond shell structure.
- Bond shell output:** A dialog box for configuring bond shell parameters such as Die, Output Layer, Start Pin Number, and SF Label.
- Net definition command:** A dialog box for defining net names and properties.
- Package DRC:** A Design Rule Check (DRC) table for package-specific rules.
- List output program:** A table listing ball locations and their associated net names.
- BGA/input and output program:** A dialog box for defining BGA input and output parameters.
- DXFOUT2:** A button for exporting the design to a DXF file.

Check Item	Execute
VBP - Resist	ON
VBP - VBP	OFF
Ball - Via Overlap	ON
Bond Wire - Bond Wires (2D)	ON
Bond Wire - Bond Wires (3D)	OFF
Bond Wire Length	OFF
VBP - Via	OFF
Bond Wire Angle from VBP	OFF
Bond Wire Angle from Die Pad	OFF
Ring - Ring	OFF
VBP - Ring	OFF
Ring Width	OFF
Bond Wire Attach Point (from Edge)	OFF
Bond Wire Attach Point (from Center)	OFF
Die Pad - Bond Wire	OFF
VBP - Bond Wire	OFF
Same Surface	OFF
BW Point - BW Point on Same VBP	OFF

Ref_Name	Pin_No.	Coord_X	Coord_Y	Net_Name
BALL0	1B	-4250.00000	-3750.00000	SIG000133
BALL0	1C	-4250.00000	-3250.00000	SIG000135
BALL0	1D	-4250.00000	-2750.00000	SIG000137
BALL0	1E	-4250.00000	-2250.00000	SIG000140
BALL0	1F	-4250.00000	-1750.00000	SIG000143
BALL0	1G	-4250.00000	-1250.00000	SIG000145
BALL0	1H	-4250.00000	-750.00000	SIG000149
BALL0	1I	-4250.00000	-250.00000	SIG000152

# 8-10 HIC design module [Optional] New

## [Function]

We have released a product consisting of commands to design a printed resistor on the Board Designer.

- The selected printed component is automatically modified or placed to a component with the appropriate shape and attribute according to the specified value.
- When a line is selected, dielectric (cross glass) is generated on a dielectric area figure layer above or below the layer containing the line.
- Each trimming probe attribute is set to each printed resistor and the probe ID attribute is set to each probe. You can check information on reallocation of probe IDs, printed resistors and probes.

